

TSMC22: 3.3V GPIO



Libraries

Name	Process	Form Factor
RGO_TSMC22_18V33_ULP_20C	ULP	Staggered CUP

Summary

The 3.3V GPIO library provides general purpose bidirectional I/O cells. These programmable, multi-voltage I/O's give the system designer the flexibility to design to a wide range of performance targets.

This library is available in a staggered CUP wire bond implementation with a flip chip option.

To design an operational I/O power domain with these cells, an additional library is required – 3.3V Support: Power. That library contains an input-only buffer, isolated analog I/O, and a full complement of power cells along with corner and spacer cells to assemble a functional pad ring by abutment. An included rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

ESD Protection:

- JEDEC compliant
 - 2kV ESD Human Body Model (HBM)
 - 500V ESD Charge Device Model (CDM)

Latch-up Immunity:

- JEDEC compliant
 - Tested to I-Test criteria of $\pm 100\text{mA}$ @ 125°C

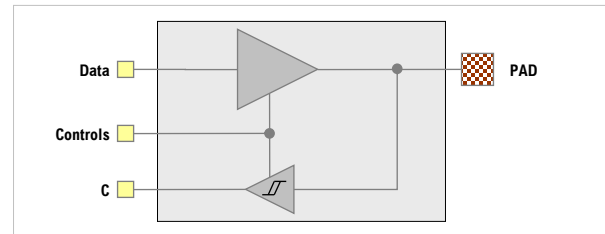
Cell Size & Form Factor

- Staggered (pad-limited) – $25\mu\text{m} \times 165\mu\text{m}$

Recommended Operating Conditions

Description	Min	Nom	Max	Units
V_{VDD} Core supply voltage	0.81	0.9	0.99	V
	1.62	1.8	1.98	V
V_{DVDD} I/O supply voltage	2.25	2.5	2.75	V
	2.97	3.3	3.63	V
T_{J} Junction temperature	-40	25	125	$^\circ\text{C}$
V_{PAD} Voltage at PAD	$V_{\text{DVSS}} - 0.3$	-	$V_{\text{DVDD}} + 0.3$	V

SRP_BI_SDS_33V_STB



Bidirectional GPIO Driver Features

- Multi-voltage (1.8V, 2.5V, 3.3V)
- LVCMOS / LVTTTL input with selectable hysteresis
- Programmable drive strength (rated 2mA to 12mA)
- Selectable output slew rate
- Optimized for EMC with SSO factor of 8
- Open-drain output mode
- Programmable input options (hi-Z/pull-up/pull-down/repeater)
- Power-On Start (POS) capable
- Power sequencing independent design with Power-On Control

In full-drive mode, this driver can operate to frequencies in excess of 100MHz with 15pF external load and 125 MHz with 10pF load. Actual frequency limits are load and system dependent. A maximum of 200 MHz can be achieved under small capacitive loads.

Characterization Corners

Nom VDD	Model	LPE	VDD	DVDD [1]	Temp
0.9V	FF	Cbest	+10%	+10%	-40 $^\circ\text{C}$
	FF	Cbest	+10%	+10%	0 $^\circ\text{C}$
	FF	Cbest	+10%	+10%	125 $^\circ\text{C}$
	FFG	Ctypical	+10%	+10%	125 $^\circ\text{C}$
	TT	Ctypical	nominal	nominal	25 $^\circ\text{C}$
	TT	Ctypical	nominal	nominal	85 $^\circ\text{C}$
	SS	Cworst	-10%	-10%	-40 $^\circ\text{C}$
	SS	Cworst	-10%	-10%	0 $^\circ\text{C}$
	SS	Cworst	-10%	-10%	125 $^\circ\text{C}$

[1] DVDD = 1.8V, 2.5V, 3.3V

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