

# GF22: 3.3V GPIO FT



AUTOMOTIVE GRADE

## Libraries

Name	Process	Form Factor
RGO_GF22_18V33_FDX_25C_FT	FDX	Staggered CUP
RGO_GF22_18V33_FDX_45C_FT	FDX	Inline CUP

## Summary

The 3.3V GPIO FT library provides general purpose bidirectional I/O cells that are fault tolerant. These programmable, multi-voltage I/O's give the system designer the flexibility to design to a wide range of performance targets.

This 22nm library is available in a staggered CUP wire bond implementation with a flip chip option.

To design a functional I/O power domain with these cells, an additional library is required – 3.3V Support: Power. That library contains an input-only buffer, isolated analog I/O, and a full complement of power cells along with corner and spacer cells to assemble a complete pad ring by abutment. An included rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

### ESD Protection:

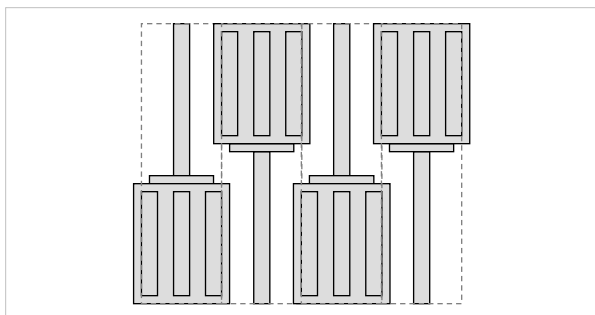
- JEDEC compliant
  - 2KV ESD Human Body Model (HBM)
  - 500 V ESD Charge Device Model (CDM)
    - 750V corner pin C4B package classification achieved by following key design priorities

### Latch-up Immunity:

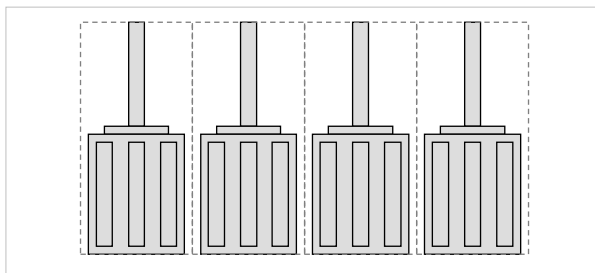
- JEDEC compliant
  - Tested to I-Test criteria of  $\pm 100\text{mA}$  @  $125^\circ\text{C}$

## Cell Size & Form Factor

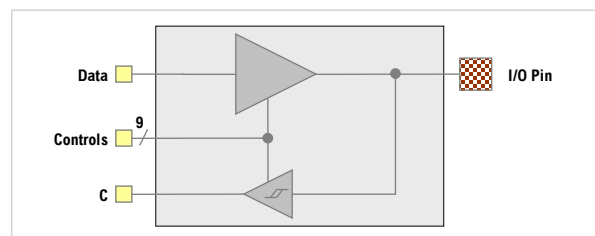
### Staggered (pad-limited) – TBD $\mu\text{m}$ x TBD $\mu\text{m}$



### Inline (core-limited) – TBD $\mu\text{m}$ x TBD $\mu\text{m}$



## FRx\_BI\_SDS\_1833V\_STB



## Bidirectional GPIO Driver Features

- Multi-Voltage (1.2V, 1.5V, 1.8V, 2.5V, 3.3V)
- LVCMOS / LVTTTL input with selectable hysteresis
- Programmable drive strength (rated 2mA to 12mA)
- Selectable output slew rate
- Optimized for EMC with SSO factor of 8
- Open-drain output mode
- Programmable input options (pull-up/pull-down/repeater)
- Power-On Start (POS) capable
- Power sequencing independent design with Power-On Control

In full-drive mode, this driver can operate to frequencies in excess of 100MHz with 15pF external load and 125 MHz with 10pF load. Actual frequency limits are load and system dependent. A maximum of 200 MHz can be achieved under small capacitive loads.

Vertical-only ( $\_V$ ) and horizontal-only ( $\_H$ ) variants provided.

## Recommended operating conditions

Description	Min	Nom	Max	Units
$V_{VDD}$ Core supply voltage	0.81	0.9	0.945	V
	0.72	0.8	0.88	V
	0.59	0.65	0.715	V
	0.45	0.5	0.55	V
$V_{DVDD}$ I/O supply voltage	2.97	3.3	3.63	V
	2.25	2.5	2.75	V
	1.62	1.8	1.98	V
	1.35	1.5	1.65	V
$T_J$ Junction temperature	-40	25	150	$^\circ\text{C}$
$V_{PAD}$ Voltage at PAD	$V_{DVSS} - 0.3$	-	$V_{DVDD} + 0.3$	V

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## Characterization Corners

Nominal VDD	Model	VDD	DVDD <sup>[1]</sup>	Temperature
0.65V (AG2)	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	TT	nominal	nominal	85°C
	SS	0.59V	-10%	-40°C
	SS	0.59V	-10%	125°C
0.8V / 0.5V (AG2)	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	TT	nominal	nominal	85°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
0.9V Overdrive (AG2)	FF	+5%	+10%	-40°C
	FF	+5%	+10%	125°C
	TT	nominal	nominal	25°C
	TT	nominal	nominal	85°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
0.8V (AG1)	FF	+5%	+10%	-40°C
	FF	+5%	+10%	125°C
	FF	+5%	+10%	150°C
	SS	-10%	-10%	150°C
	SS	-10%	-10%	150°C

[1] DVDD = 1.2V, 1.5V, 1.8V, 2.5V & 3.3V

**NOTE:** I/O cell performance characteristics are guaranteed only from  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$ . Up to  $T_J = 150^\circ\text{C}$ , the cells are only guaranteed to be operational.

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