GF22: SD

Libraries

Name	Process	Form Factor
RGO_GF22_18V33_FDX_20C_SD	FDX	Staggered CUP

Summary

The SD library provides bidirectional SD 3.0 signaling cells. It is compatible with revision 3.01 of the SD Specifications, Part 1, Physical Layer Specification. It is also compatible with the Embedded Multi-Media Card (eMMC) Electrical Standard (5.1) (JESD84-B51 – February 2015). This library is offered as a supplement to the standard GPIO libraries provided by Aragio Solutions.

This 22nm library is available in a staggered CUP wire bond implementation with a flip chip option.

To utilize these cells in the pad ring, an additional library is required – 3.3V Support: Power. That library contains the necessary power cells, the POC and VREF cells, and a rail splitter to isolate the SD cells in their own power domain as recommended. It also contains an input-only buffer, isolated analog I/O, and a full complement of power cells along with corner and spacer cells to assemble a complete pad ring by abutment. The rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

ESD Protection:

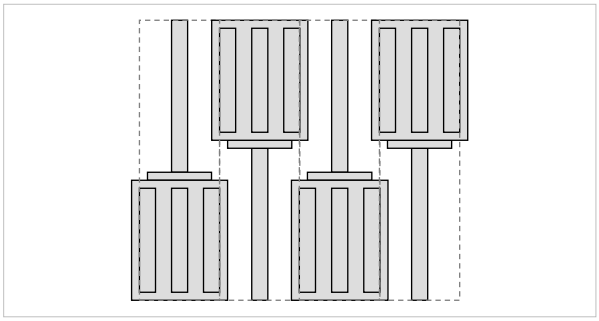
- JEDEC compliant
  - 2KV ESD Human Body Model (HBM)
  - 500 V ESD Charge Device Model (CDM)

Latch-up Immunity:

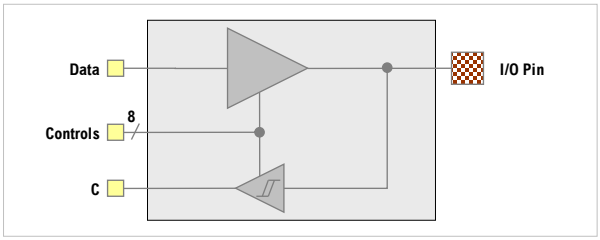
- JEDEC compliant
  - Tested to I-Test criteria of ± 100mA @ 125°C

Cell Size & Form Factor

Staggered (pad-limited) – TBDμm x TBDμm



STP_BI_016_1833V_SD3



Bidirectional SD 3.0 Driver Features

- Dual voltage operation (1.8V & 3.3V)
- Programmable drive strength
- Selectable output slew-rate (slow / fast)
- Selectable schmitt trigger input
- Programmable input options (pull-up, pull-down, or plain input)
- Fully compatible with Aragio Solutions 3.3V I/O library offerings
- Power-up sequencing independent design with Power-on Control

Vertical-only (_V) and and horizontal-only (_H) variants provided.

Recommended operating conditions

	Description		Min	Nom	Max	Units
V_{VDD}	Core supply voltage		0.72	0.8	0.88	V
T_J	Junction temperature		-40	25	+125	°C
V_{PAD}	Voltage at IO		-0.3		V_{DVDD} + 0.3	V
V_{DVDD}	I/O supply voltage	3.3V	2.7	3.3	3.63	V
V_{IH}	Input logic high	3.3V	0.625 * V_{DVDD}	-	V_{DVDD} + 0.3	V
V_{IL}	Input logic low	3.3V	V_{DVSS} - 0.3	-	0.25 * V_{DVDD}	V
V_{HYS}[1]	Input hysteresis voltage	3.3V	0.2	-	-	V
V_{DVDD}	I/O supply voltage	1.8V	1.7	1.8	1.95	V
V_{IH}	Input logic high	1.8V	0.65 * V_{DVDD}	-	V_{DVDD} + 0.3	V
V_{IL}	Input logic low	1.8V	V_{DVSS} - 0.3	-	0.35 * V_{DVDD}	V
V_{HYS} [1]	Input hysteresis voltage	1.8V	0.1 * V_{DVDD}	-	-	V

[1] When SMT = 1.

Characterization Corners

Nominal VDD	Model	VDD	DVDD[1]	Temperature
0.8V	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	TT	nominal	nominal	85°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C

[1] DVDD = 1.8V, 3.0 & 3.3V