

Libraries

Name	Process	Form Factor
RGO_GF28_50V50_SLP_25C_I2C	SLP	Staggered

Summary

Conforms to UM10204 I2C-bus specification and user manual, Rev.4 – 13 February 2012, NXP

The I2C I/O pad is an open-drain bi-directional I/O cell that is designed for the I2C two-line interface. Utilized with the 3.3V GPIO library, it is compliant with the I2C-bus specification.

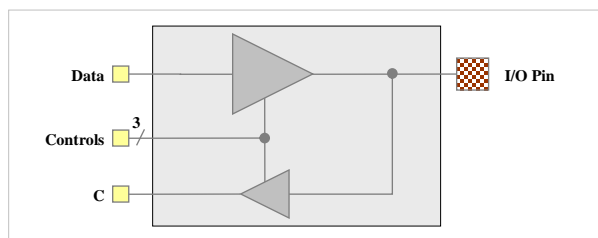
The I2C cell is designed for 100Kbps and 400 Kbps operation.

An open-drain design, this cell requires an external pull-up resistor to a high voltage power supply. The pull-up power supply (VDDP) for this design is between 4.50V to 5.50V. It is independent of the I/O cell power supply (DVDD). The sizing of the external resistor is application dependent and can range from 1.7 K Ω to 40 K Ω .

Product Features

- Supported I2C operating modes:
 - Standard-mode (Sm) – 100 Kbps data rate
 - Fast mode (Fm) – 400 Kbps data rate
- Open drain operation only (floating NWELL with PMOS used for ESD protection only)
- Built-in output slew rate control to meet I²C T_{of} minimum of (20 x VDDP/5.5V) ns
- Output enable
- Receiver enable
- ESD protection uses snap-back devices (no diode to the positive power supply)
- Standard LVCMOS input thresholds with Schmidt trigger (hysteresis) option
- Staggered I/O CUP implementation
- Power-on sequencing independent design with Power-On Control
- DVDD = 2.97V to 3.63V and VDD = 0.90V to 1.155V
- Pad VDDP (power supply reference for Output) = 4.50V to 5.50V independent of DVDD.
- The circuit consumes no DC supply current in the static state

I2P_ON_003_5T_NC



Recommended operating conditions

Description	Min	Nom	Max	Units
V _{DVDD} I/O supply voltage	2.70	3.3	3.63	V
V _{VDDP} External pull-up supply to PAD	2.70	3.3	3.63	V
V _{VDD} Core supply voltage	0.90	1.0	1.10	V
	0.99	1.1	1.155	V
T _J Junction temperature	-40	25	125	°C
V _{PAD} Voltage at PAD	V _{DVSS} – 0.3	-	V _{VDDP}	V

ESD Protection:

- JEDEC compliant
 - 2KV ESD Human Body Model (HBM)
 - 200V ESD Machine Model (MM)
 - 500V ESD Charge Device Model (CDM)

Latch-up Immunity:

- JEDEC compliant
 - Tested to I-Test criteria of $\pm 100\text{mA}$ @ 125°C

Characterization Corners

Nominal VDD	Model	VDD	DVDD = 3.3V	Temperature
1.1	FF	+5%	+10%	-40°C
	FF	+5%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
	1.0	FF	+10%	+10%
FF		+10%	+10%	125°C
TT		nominal	nominal	25°C
SS		-10%	-10%	-40°C
SS		-10%	-10%	125°C

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Aragio Solutions
2201 K Avenue
Section B Suite 200
Plano, TX 75074-5918
Phone: (972) 516-0999
Fax: (972) 516-0998
Web: <http://www.aragio.com/>

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