

## Libraries

Name	Process	Form Factor
RGO_SMIC28_18V33_HKCP_40C_RF	HKC+	Inline CUP

## Summary

The RF library provides Analog / RF I/O cells including LNA input pads, a 5V tolerant PA output pad and a 10GHz analog signal pad with multiple input resistance options. Discrete components (RF diodes and SCR's) are provided to enable construction of a custom ESD protection solution.

These 28nm libraries are available in an inline CUP wire bond implementation with a flip chip option.

### ESD Protection:

- JEDEC compliant
  - 2KV ESD Human Body Model (HBM)
  - 500 V ESD Charge Device Model (CDM)

### Latch-up Immunity:

- JEDEC compliant
  - Tested to I-Test criteria of  $\pm 100\text{mA}$  @  $125^\circ\text{C}$

## RF Diodes

A set of PPLUS\_NWELL\_DIODE RF diodes provide minimum capacitance for RF applications and high current handling capability for good ESD protection.

## Silicon-Controlled Rectifiers (SCR)

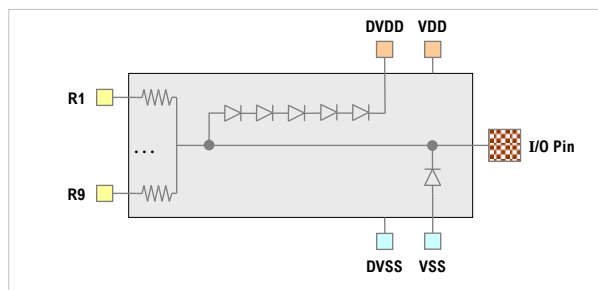
A set of P+ to Nwell SCR discrete components provide the lowest capacitance with the highest ESD protection. These components have been used in I/O pads to demonstrate over 6KV ESD protection.

## ANC\_BI\_DWR\_5T

ANC\_BI\_DWR\_5T is a 10 GHz bi-directional analog (thick gate) signal pad with selectable input resistance. Resistors R1 to R4 and R6 to R9 can be used in parallel to achieve the desired resistance value as low as 1.3 ohms.

This structure can then be used with output amplifiers for which R5 can be used in the feedback path. If used in this manner, R1 to R4 and R6 to R9 should be individually connected to isolated fingers of the driver transistors.

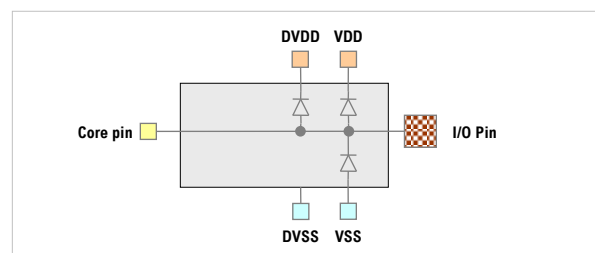
The stacked diode ESD structure from DVDD to the I/O pin provides extended overvoltage protection.



## Analog / RF Pads

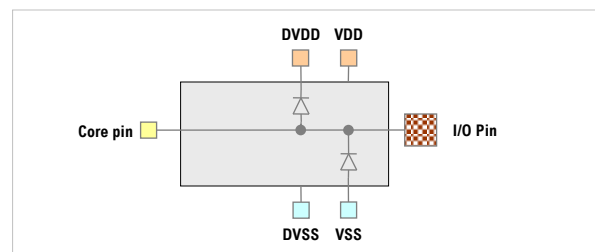
### ANC\_IN\_LNA\_1033V

ANC\_IN\_LNA\_10V is a 0 to 1.1V analog I/O pad optimized for low capacitance and designed to protect thin gate oxide input devices. The layout uses wide metal 3 interconnect (14  $\mu\text{m}$ ) for low inductance from the bond pad to the core.



### ANC\_IN\_LNA\_33V

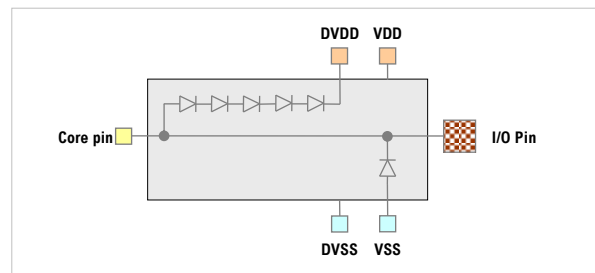
ANC\_IN\_LNA\_33V is a 0 to 3.3V analog I/O pad optimized for low capacitance. The layout uses wide metal 3 interconnect (12  $\mu\text{m}$ ) for low inductance from the bond pad to the core.



### ANC\_OU\_PWA\_5T

ANP\_OU\_PWA\_5T is an analog I/O pad optimized for low capacitance which uses SCRs for ESD clamp devices.

The stacked diode ESD structure from DVDD to the I/O pin provides extended overvoltage protection. With a 3.3V power supply, this I/O pad is 5V tolerant. Dropping to an I/O domain power supply of 1.8V, the pad is 3.3V tolerant.



## Recommended operating conditions

Description	Min	Nom	Max	Units
V <sub>VDD</sub> Core supply voltage	0.81	0.90	0.99	V
	2.97	3.3	3.63	V
V <sub>DVDD</sub> I/O supply voltage	2.25	2.5	2.75	V
	1.62	1.8	1.98	V
T <sub>J</sub> Junction temperature	-40	25	125	°C
V <sub>PAD</sub> Voltage at PAD <sup>[1]</sup>	V <sub>DVSS</sub> -0.3	-	V <sub>DVDD</sub> +0.3	V

[1] The DWR\_5T & PWA\_5T cells are 5V tolerant @ 3.3V and 3.3V tolerant @ 1.8V

## Characterization Corners

Model	LPE Type	VDD=0.9V	DVDD <sup>[1]</sup>	Temp
FFG	Cbest	+10%	+10%	-40°C
FFG	Cbest	+10%	+10%	0°C
FFG	Ctypical	+10%	+10%	125°C
TT	Ctypical	nominal	nominal	25°C
TT	Ctypical	nominal	nominal	85°C
SSG	Cworst	-10%	-10%	-40°C
SSG	Cworst	-10%	-10%	0
SSG	Cworst	-10%	-10%	125°C

[1] DVDD = 1.8V, 2.5V & 3.3V

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