TSMC 05: I2C

Libraries

Name	Process	Form Factor
RGO_TSMC05_15V18_N5_45F_I2C	N5	Inline

Summary

The I2C library provides an open-drain bi-directional I/O driver designed for the I²C two-line interface. It is compliant with the I²C-bus specification – UMC10204 I²C-bus specification and user manual, Rev. 6 – 04 April 2014, NXP.

The design supports the Sm, Fm, Fm+, and Hs modes of operation at the I²C bus operating voltage (VDDP) of 1.8V.

This 5nm library is available in an inline flip chip implementation.

To design a functional I/O power domain with this cell, an additional library is required – 1.8V Support: Power. That library contains isolated analog I/O, and a full complement of power cells along with spacer cells to assemble a complete pad ring by abutment. An included rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

ESD Protection:

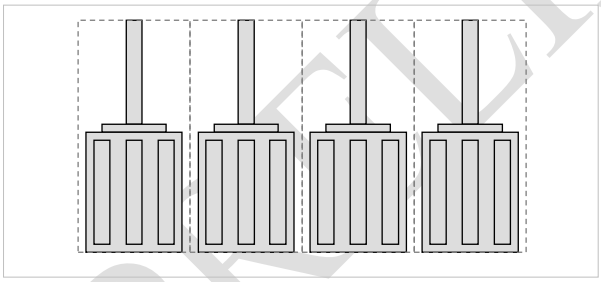
- JEDEC compliant
  - 2KV ESD Human Body Model (HBM)
  - 500 V ESD Charge Device Model (CDM)

Latch-up Immunity:

- JEDEC compliant
  - Tested to I-Test criteria of ± 100mA @ 125°C

Cell Size & Form Factor

Inline (core-limited) – 99.82µm x 100.1µm

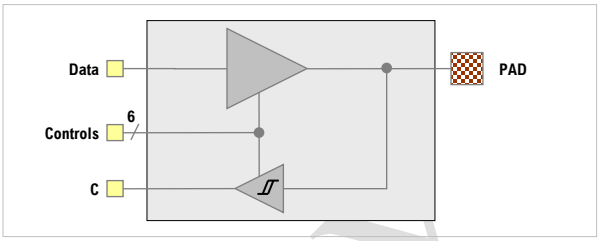


Orientation-limited cells are only provided in the vertical-only (_V) orientation.

Recommended operating conditions

	Description	Min	Nom	Max	Units
V_{DVDD}	I/O supply voltage	1.62	1.8	1.98	V
V_{VDDP}	External pull-up supply to PAD	1.62	1.8	1.98	V
V_{VDD}	Core supply voltage	0.675	0.75	0.825	V
		0.765	0.85	0.935	V
T_J	Junction temperature	-40	25	125	°C
V_{PAD}	Voltage at PAD	V_{DVSS} – 0.3	-	1.98	V

I2C_ON_003_18V_NC



I²C Bi-directional Driver Features

- Supported I2C operating modes:
  - Standard-mode (Sm) – 100 Kbps data rate
  - Fast mode (Fm) – 400 Kbps data rate
  - Fast mode (Fm+) – 1.0 Mbps data rate
  - High-speed mode (Hs) - 3.4 Mbps data rate
- Open drain operation only
- Built-in output slew rate control to meet I²C T_{of} minimum of (20 x VDDP/5.5V) ns
- Output enable and mode select
- Receiver enable
- ESD protection is accomplished with an SCR (no diode to the positive power supply)
- Standard LVCMOS compatible input with optional Schmitt trigger (hysteresis)
- Power-on sequencing independent design with Power-On Control
- DVDD = 1.62V to 1.98V
- Pad VDDP = 1.62V to 1.98V – independent of DVDD
- The circuit consumes no DC supply current in the static state
- Fault-tolerant to 1.98V at PAD (no current flow when DVDD = 0V)

An open-drain design, this cell requires an external pull-up resistor to a high voltage power supply. Designed for a 1.8V I²C bus application, VDDP can track DVDD but it is not necessary. The sizing of the external resistor or appropriate pull-up network is application dependent.

Characterization Corners

Model	LPE Type	VDD [1]	DVDD [2]	Temp
FFGNP	Cbest_CCbest	+10%	+10%	-40°C
FFGNP	Cbest_CCbest	+10%	+10%	0°C
FFGNP	Cbest_CCbest	+10%	+10%	125°C
TT	Ctypical	nominal	nominal	25°C
TT	Ctypical	nominal	nominal	85°C
SSGNP	Cworst_CCworst	-10%	-10%	-40°C
SSGNP	Cworst_CCworst	-10%	-10%	0°C
SSGNP	Cworst_CCworst	-10%	-10%	125°C

[1] VDD = 0.75V & 0.85V
[2] DVDD = 1.8V

Published by:

Aragio Solutions
2201 K Avenue
Section B Suite 200
Plano, TX 75074-5918
Phone: **(972) 516-0999**
Fax: **(972) 516-0998**
Web: http://www.aragio.com/

Printed in the United States of America