

Libraries

Name	Process	Form Factor
RGO_TSMC05_15V18_N5_45F_I3C	N5	Inline

Summary

The I3C library provides a bi-directional I/O driver designed for the I3C two-line interface. It is compliant with the MIPI Specification for I3C –Version 1.1, 27 November 2019.

The design supports the IC3 push-pull and open-drain modes as well as legacy Fm and Fm+ open-drain modes at the bus operating voltages of 1.2V and 1.8V.

This 5nm library is available in an inline flip chip implementation.

To design a functional I/O power domain with this cell, an additional library is required – 1.8V Support: Power. That library contains isolated analog I/O, and a full complement of power cells along with spacer cells to assemble a complete pad ring by abutment. An included rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

ESD Protection:

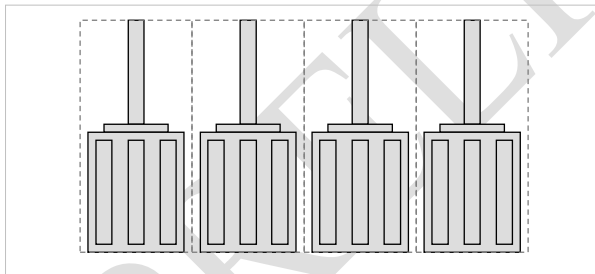
- JEDEC compliant
 - 2KV ESD Human Body Model (HBM)
 - 500 V ESD Charge Device Model (CDM)

Latch-up Immunity:

- JEDEC compliant
 - Tested to I-Test criteria of $\pm 100\text{mA}$ @ 125°C

Cell Size & Form Factor

Inline (core-limited) – $99.82\mu\text{m} \times 100.1\mu\text{m}$

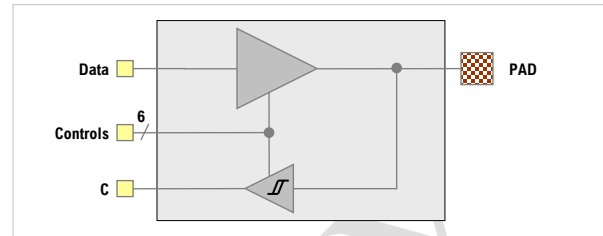


Orientation-limited cells are only provided in the vertical-only (_V) orientation.

Recommended operating conditions

Description	Min	Nom	Max	Units
V_{DVDD} I/O supply voltage	1.10	1.2	1.30	V
	1.65	1.8	1.95	V
V_{VDDP} External pull-up supply to PAD	1.10	1.2	1.30	V
	1.65	1.8	1.95	V
V_{VDD} Core supply voltage	0.675	0.75	0.825	V
	0.765	0.85	0.935	V
T_J Junction temperature	-40	25	125	$^\circ\text{C}$
V_{PAD} Voltage at PAD	$V_{DVSS} - 0.3$	-	1.98	V

I3C_ON_003_18V_NC



I3C Bi-directional Driver Features

- Supported I3C operating modes:
 - I3C push-pull mode – up to 12.5 MHz
 - I3C open-drain mode – up to 12.5 Mbps data rate
 - Legacy Fast mode (Fm) – up to 400 Kbps data rate
 - Legacy Fast mode (Fm+) – up to 1.0 Mbps data rate
- Output enable and mode select
- Receiver enable
- Standard LVCMOS compatible input with optional Schmitt trigger (hysteresis)
- ESD protection is accomplished with stacked NMOS breakdown devices
- Power-on sequencing independent design with Power-On Control
- $DVDD = 1.2\text{V}$ or 1.8V
- Pad $VDDP$ (open-drain) = 1.65V to 1.95V or 1.20V to 1.30V – independent of $DVDD$
- The circuit consumes no DC supply current in the static state in the open-drain modes
- Fault-tolerant to 1.98V at PAD (no current flow when $DVDD = 0\text{V}$)

In open-drain modes, this cell requires a pull-up to a high voltage power supply ($VDDP$). The sizing of an external resistor or appropriate pull-up network is application dependent.

Characterization Corners

Model	LPE Type	VDD [1]	DVDD [2]	Temp
FFGNP	Cbest_CCbest	+10%	+10%	-40 $^\circ\text{C}$
FFGNP	Cbest_CCbest	+10%	+10%	0 $^\circ\text{C}$
FFGNP	Cbest_CCbest	+10%	+10%	125 $^\circ\text{C}$
TT	Ctypical	nominal	nominal	25 $^\circ\text{C}$
TT	Ctypical	nominal	nominal	85 $^\circ\text{C}$
SSGNP	Cworst_CCworst	-10%	-10%	-40 $^\circ\text{C}$
SSGNP	Cworst_CCworst	-10%	-10%	0 $^\circ\text{C}$
SSGNP	Cworst_CCworst	-10%	-10%	125 $^\circ\text{C}$

[1] $VDD = 0.75\text{V}$ & 0.85V

[2] $DVDD = 1.8\text{V}$

PRELIMINARY

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