

Libraries

Name	Process	Form Factor
RGO_TSMC07_18V18_7FF_20C_ONFI_4_1	7FF	Staggered

Summary

The ONFI 4.1 library provides the combo driver / receiver cells, the ODT / driver impedance calibration cell, and the voltage reference cell to support both single-ended and differential ONFI 4.1 signaling. This library also meets the requirements for ONFI 3.0 & Toggle 2.0 signaling. Also included is a full complement of power, spacer, and adapter cells to assemble a complete pad ring by abutment. An included rail splitter allows isolated ONFI domains to be placed in the same pad ring with other power domains while maintaining continuous VDD/VSS in the pad ring for robust ESD protection.

The ONFI 4.1 I/O library supports all impedance modes defined in the ONFI 4.1 specification and features fast and precise calibration, low power consumption, area-efficient design, and easy integration into the physical layer (PHY).

This 7nm library is available in a staggered flip chip implementation.

ESD Protection:

- JEDEC compliant
 - 2KV ESD Human Body Model (HBM)
 - 500 V ESD Charge Device Model (CDM)

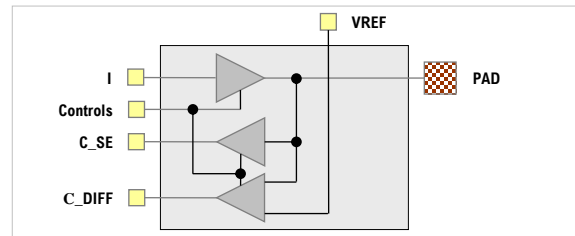
Latch-up Immunity:

- JEDEC compliant
 - Tested to I-Test criteria of $\pm 100\text{mA}$ @ 125°C

Cell Size & Form Factor

- Staggered (pad-limited) – $\text{TBD}\mu\text{m} \times \text{TBD}\mu\text{m}$

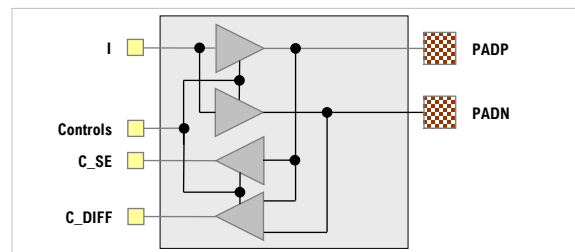
ONP_BI_SDS_1218V_SCB: Single-Ended Driver



ONFI Single-Ended Driver / Receiver Features:

- Driver – user-selectable on-die termination and programmable drive strength with ODT / Z_O calibration and programmable “off” state control.
 - $\text{ODT } R_{it} = 30\Omega / 50\Omega / 75\Omega / 100\Omega / 150\Omega$
 - $Z_{OUT} = 18\Omega / 25\Omega / 35\Omega / 50\Omega$
 - Off state – Z / pull-up / pull-down / bus keeper
- Receiver – single-ended and pseudo-differential outputs
- Powered by 1.2V / 1.8V I/O and 0.8V core supplies
- Maximum operating frequency – 400 MHz

ONP_CL_SDS_1218V_SCB: Differential Driver



ONFI Differential Clock Driver / Receiver Features:

- Driver – user-selectable on-die termination and programmable drive strength with ODT / Z_O calibration and programmable “off” state control.
 - $\text{ODT } R_{it} = 30\Omega / 50\Omega / 75\Omega / 100\Omega / 150\Omega$
 - $Z_{OUT} = 18\Omega / 25\Omega / 35\Omega / 50\Omega$
 - Off state – Z / pull-up / pull-down / bus keeper
- Receiver – single-ended and true differential outputs
- Powered by 1.2V / 1.8V I/O and 0.8V core supplies
- Maximum operating frequency – 400 MHz

Recommended operating conditions

Symbol	Description	Min	Nom	Max	Units
V _{VDD}	Core supply voltage	0.675	0.75	0.825	V
		0.765	0.85	0.935	V
T _J	Junction temperature	-40	25	125	°C
V _{PAD}	Voltage at PAD	-0.3V		V _{DVDD} +0.3V	V
V _{DVDD}	I/O supply voltage	1.62	1.8	1.98	V
V _{IH(DC)}	Input High (DC)	0.7 * V _{DVDD}		V _{DVDD} + 0.3	V
V _{IL(DC)}	Input Low (DC)	V _{DVSS} - 0.3		0.3 * V _{DVDD}	V
V _{IH(AC)}	Input High (AC)	0.8 * V _{DVDD}		V _{DVDD} + 0.3	V
V _{IL(AC)}	Input Low (AC)	V _{DVSS} - 0.3		0.2 * V _{DVDD}	V
V _{DVDD}	I/O supply voltage	1.62	1.8	1.98	V
V _{IH(DC)}	Input High (DC)	V _{REF} +.125		V _{DVDD} + 0.3	V
V _{IL(DC)}	Input Low (DC)	V _{DVSS} - 0.3		V _{REF} -.125	V
V _{IH(AC)}	Input High (AC)	V _{REF} +.250			V
V _{IL(AC)}	Input Low (AC)			V _{REF} -.125	V
V _{DVDD}	I/O supply voltage	1.14	1.2	1.26	V
V _{IH(DC)}	Input High (DC)	V _{REF} +.100		V _{DVDD} + 0.3	V
V _{IL(DC)}	Input Low (DC)	V _{DVSS} - 0.3		V _{REF} -.100	V
V _{IH(AC)}	Input High (AC)	V _{REF} +.150			V
V _{IL(AC)}	Input Low (AC)			V _{REF} -.150	V

Characterization Corners *

Model	LPE Type	VDD [1]	DVDD	Temp
FF	Cbest_CCbest	+10%		-40°C
FF	Cbest_CCbest	+10%		125°C
TT	Ctypical	nominal	See table below for DVDD voltage ranges.	25°C
TT	Ctypical	nominal		85°C
SS	Cworst_CCworst	-10%		-40°C
SS	Cworst_CCworst	-10%		125°C

[1] VDD = 0.75V
* PRELIMINARY

Library Characterization DVDD Voltage Ranges

Nominal DVDD		FF	TT	SS	Units
1.8	NV-DDR & NV-DDR2	1.95	1.8V	1.7	V
1.2	NV-DDR3	1.26	1.2	1.14	V

Cell summary

Name	Description
ONP_BI_SDS_1218V_SCB *	ONFI Single-Ended Driver/Receiver
ONP_CL_SDS_1218V_SCB *	ONFI Differential Clock Driver/Receiver
ONP_SP_CAL_1218V *	Calibration cell
ONP_RE_000_1218V *	Voltage Reference (VREF).
PVP_VD_PDO_1218V *	I/O V _{DD} (DVDD) with POC
PVP_VD_RDO_1218V *	I/O V _{DD} (DVDD)
PVP_VS_RDO_1218V *	I/O V _{SS} (DVSS)
PVP_VS_DRC_1218V *	I/O V _{SS} (DVSS is shorted to VSS)
PVP_VD_RCD_0918V *	Core V _{DD} (VDD)
PVP_VS_RCD_0918V *	Core V _{SS} (VSS)
PVP_VS_DRC_0918V *	Core V _{SS} (DVSS is shorted to VSS)
SVP_CO_000_1218V	Corner cell – rail splitter
SVP_CO_001_1218V	Corner cell - continous
SVP_SP_001_1218V	1µm spacer cell
SVP_SP_005_1218V *	5µm spacer cell
SVP_SP_020_1218V *	20µm spacer cell
SPP_RS_005_1218V	Rail splitter cell
SPP_SP_CAP_1218V	Core decoupling cap cell

* Vertical-only and horizontal-only orientations

Staggered CUP Cells

CUP_TSMC16_44X80_IN	44µm X 80µm Inner
CUP_TSMC16_44X80_OUT	44µm X 80µm Outer
CUP_TSMC16_FC	Flip chip with top metal port
CUP_TSMC16_FC_NRV	Flip chip without RV vias

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