

TSMC 07: 1.8V 100MHz Oscillator



Libraries

Name	Process	Form Factor
RGO_TSMC07_18V18_7FF_20C_OSC	7FF	Staggered

Summary

The 1.8V 100 MHz Oscillators library contains oscillator macro I/O cells.

This 7nm library is available in a staggered flip chip implementation.

To utilize these cells in the pad ring, an additional library is required – 1.8V Support: Power. That library contains the DVDD/DVSS power cells necessary for ESD protection, the POC cell, and a rail splitter to isolate the oscillator in its own power domain as recommended. It also contains an input-only buffer, isolated analog I/O, and a full complement of power cells along with corner and spacer cells to assemble a complete pad ring by abutment. The rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

ESD Protection:

- JEDEC compliant
 - 2KV ESD Human Body Model (HBM)
 - 500 V ESD Charge Device Model (CDM)

Latch-up Immunity:

- JEDEC compliant
 - Tested to I-Test criteria of $\pm 100\text{mA}$ @ 125°C

Cell Size & Form Factor

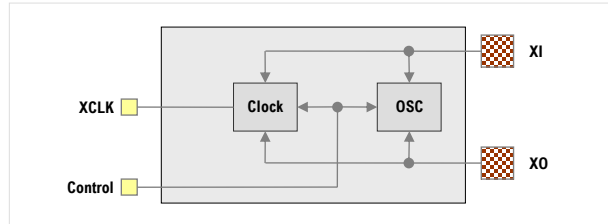
- Staggered (pad-limited) – $68.16\mu\text{m} \times 191.28\mu\text{m}$

Recommended operating conditions

Description	Min	Nom	Max	Units
V_{VDD} Core supply voltage	0.675	0.75	0.825	V
	0.765	0.85	0.935	V
	1.62	1.8	1.98	V
V_{DVDD} I/O supply voltage	1.35	1.5	1.65	V
	1.08	1.2	1.32	V
T_{J} Junction temperature	-40	25	125	$^\circ\text{C}$
V_{PAD} Voltage at X1 [1]	0	-	V_{DVDD}	V

[1] X1 can be driven by an external clock for bypass operation. XO should never be driven or loaded by anything other than the oscillator crystal.

OSP_BI_100_18V



100 MHz Oscillator Features

- Wide frequency range – 1 MHz to 100 MHz using industry standard external crystals.
- Optimized for stability and minimum jitter
- Power-down mode
- Operates on core power only (VDD/VSS cells embedded)
- In a forced bypass mode, the XI port can be driven by an I/O-level (V_{DVDD}) clock signal.

Vertical-only (_V) and horizontal-only (_H) variants provided.

Characterization Corners *

Model	LPE Type	VDD [1]	DVDD [2]	Temp
FF	Cbest_CCbest	+10%	+10%	-40 $^\circ\text{C}$
FF	Cbest_CCbest	+10%	+10%	125 $^\circ\text{C}$
TT	Ctypical	nominal	nominal	25 $^\circ\text{C}$
TT	Ctypical	nominal	nominal	85 $^\circ\text{C}$
SS	Cworst_CCworst	-10%	-10%	-40 $^\circ\text{C}$
SS	Cworst_CCworst	-10%	-10%	125 $^\circ\text{C}$

[1] VDD = 0.75V & 0.85V

[2] DVDD = 1.2V, 1.5V & 1.8V

* PRELIMINARY

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