# TSMC 07: 1.8V Support: Power

## Libraries

| Name | Process | Form Factor |
|---|---|---|
| RGO_TSMC07_18V18_7FF_20C_SPT | 7FF | Staggered |
| RGO_TSMC07_18V18_7FF_45C_SPT | 7FF | Inline |

## Summary

The 1.8V Support: Power library provides a full complement of cells to support the assembly of a complete pad ring by abutment. It is supplied as a standard addition to the GPIO libraries and other I/O library offerings from Aragio Solutions that use a compatible pad ring bus structure.

These 7nm libraries are available in inline and staggered flip chip implementations.

The included rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

**ESD Protection:**

- JEDEC compliant
  - 2KV ESD Human Body Model (HBM)
  - 500 V ESD Charge Device Model (CDM)

**Latch-up Immunity:**

- JEDEC compliant
  - Tested to I-Test criteria of ± 100mA @ 125°C

## Cell Size & Form Factor

- Staggered (pad-limited) – 17.04µm x 191.28µm
- Inline (core-limited) – TBDµm x TBDµm

## Recommended operating conditions

| | Description | Min | Nom | Max | Units |
|---|---|---|---|---|---|
| $V_{VDD}$ | Core supply voltage | 0.675 | 0.75 | 0.825 | V |
| | | 0.765 | 0.85 | 0.935 | V |
| $V_{DVDD}$ | I/O supply voltage | 1.62 | 1.8 | 1.98 | V |
| | | 1.35 | 1.5 | 1.65 | V |
| | | 1.08 | 1.2 | 1.32 | V |
| $T_J$ | Junction temperature | -40 | 25 | 125 | °C |
| $V_{PAD}$ | Voltage at PAD | $V_{DVSS}$ -0.3 | - | $V_{DVDD}$ +0.3 | V |

## Characterization Corners *

| Model | LPE Type | VDD [1] | DVDD [2] | Temp |
|---|---|---|---|---|
| FF | Cbest_CCbest | +10% | +10% | -40°C |
| FF | Cbest_CCbest | +10% | +10% | 125°C |
| TT | Ctypical | nominal | nominal | 25°C |
| TT | Ctypical | nominal | nominal | 85°C |
| SS | Cworst_CCworst | -10% | -10% | -40°C |
| SS | Cworst_CCworst | -10% | -10% | 125°C |

[1] VDD = 0.75V & 0.85V
[2] DVDD = 1.2V, 1.5V & 1.8V
* PRELIMINARY

## Cell List

| Name | Description |
|---|---|
| **Digital Pads *** | |
| STx_IN_001_18V_NC | Input-only buffer |
| **I/O Power / Ground Pads *** | |
| PWx_VD_PDO_18V | I/O power (DVDD) with POC |
| PWx_VD_RDO_18V | I/O power (DVDD) |
| PWx_VS_RDO_18V | I/O ground (DVSS) |
| PWx_VS_DRC_18V | Common ground with I/O ESD |
| **Core Power / Ground Pads *** | |
| PWx_VD_RCD_10V | Core power (VDD) |
| PWx_VS_RCD_10V | Core ground (VSS) |
| PWx_VS_DRC_10V | Common ground with Core ESD |
| **Analog Pads *** | |
| ANx_BI_DWR_18V | 1.8V Analog Input cell |
| ANx_BI_DWR_10V | 0.8V Analog Input cell |
| **Analog Power / Ground Pads *** | |
| PWx_VD_ANA_10V | Analog power (AVDD) 0.8V |
| PWx_VS_ANA_10V | Analog ground (AVSS) |
| PWx_VD_ANA_18V | Analog power (ADVDD) 1.8V |
| PWx_VS_ANA_18V | Analog ground (ADVSS) |
| **Support Pads** | |
| SPx_CO_000_18V | Corner cell (rail splitter) |
| SPx_CO_001_18V | Corner cell (continuous) |
| SPx_SP_000_18V | 0.1µm spacer |
| SPx_SP_001_18V | 1µm spacer |
| SPx_SP_005_18V | 5µm spacer |
| SPx_SP_010_18V | 10µm spacer |
| SPx_RS_005_18V | Rail splitter |

* Vertical-only (_V) and horizontal only(_H) variants provided
Cell names / descriptions abbreviated

| Staggered CUP Cells | |
|---|---|
| CUP_TSMC07_FC | Flip chip with top metal port |
| CUP_TSMC07_FC_NRV | Flip chip without RV via |

| Inline CUP Cells | |
|---|---|
| CUP_TSMC07_FC_INLINE | Flip chip with top metal port |
| CUP_TSMC07_FC_INLINE_NRV | Flip chip without RV via and RDL port |

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