

Libraries

Name	Process	Form Factor
RGO_TSMC07_18V33_7FF_20C	7FF	Staggered
RGO_TSMC07_18V33_7FF_45C	7FF	Inline

Summary

The 3.3V GPIO library provides general purpose bidirectional I/O cells. These programmable, multi-voltage I/O's give the system designer the flexibility to design to a wide range of performance targets.

These 7nm libraries are available in inline and staggered flip chip implementations.

To design a functional I/O power domain with these cells, an additional library is required – 3.3V Support: Power. That library contains an input-only buffer, isolated analog I/O, and a full complement of power cells along with corner and spacer cells to assemble a complete pad ring by abutment. An included rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

ESD Protection:

- JEDEC compliant
 - 2KV ESD Human Body Model (HBM)
 - 500 V ESD Charge Device Model (CDM)

Latch-up Immunity:

- JEDEC compliant
 - Tested to I-Test criteria of $\pm 100\text{mA}$ @ 125°C

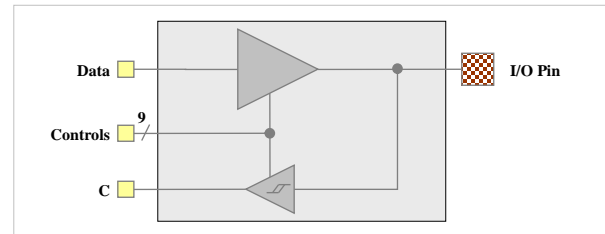
Cell Size & Form Factor

- Staggered (pad-limited) – 34.08 μm x 214.68 μm
- Inline (core-limited) – TBD μm x TBD μm

Recommended operating conditions

Description	Min	Nom	Max	Units
V _{VDD} Core supply voltage	0.675	0.75	0.825	V
	0.765	0.85	0.935	V
V _{DVDD} I/O supply voltage	2.97	3.3	3.63	V
	2.25	2.5	2.75	V
	1.62	1.8	1.98	V
	1.08	1.2	1.32	V
T _J Junction temperature	-40	25	125	°C
V _{PAD} Voltage at PAD	V _{DVSS} -0.3	-	V _{DVDD} +0.3	V

SRx_BI_SDS_1833V_STB



Bidirectional GPIO Driver Features

- Multi-Voltage (1.2V, 1.8V, 2.5V, 3.3V)
- LVCMOS / LVTTTL input with selectable hysteresis
- Programmable drive strength (rated 2mA to 12mA)
- Selectable output slew rate
- Optimized for EMC with SSO factor of 8
- Open-drain output mode
- Programmable input options (pull-up/pull-down/repeater)
- Power-On Start (POS) capable
- Power sequencing independent design with Power-On Control

In full-drive mode, this driver can operate to frequencies in excess of 100MHz with 15pF external load and 125 MHz with 10pF load. Actual frequency limits are load and system dependent. A maximum of 200 MHz can be achieved under small capacitive loads.

Vertical-only (_V) and horizontal-only (_H) variants provided.

Characterization Corners *

Model	LPE Type	VDD [1]	DVDD [2]	Temp
FF	Cbest_CCbest	+10%	+10%	-40°C
FF	Cbest_CCbest	+10%	+10%	125°C
TT	Ctypical	nominal	nominal	25°C
TT	Ctypical	nominal	nominal	85°C
SS	Cworst_CCworst	-10%	-10%	-40°C
SS	Cworst_CCworst	-10%	-10%	125°C

[1] VDD = 0.75V & 0.85V

[2] DVDD = 1.2V, 1.8V, 2.5V & 3.3V

* PRELIMINARY

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