

TSMC 07: 3.3V Support: Power



Libraries

Name	Process	Form Factor
RGO_TSMC07_18V33_7FF_20C_SPT	7FF	Staggered
RGO_TSMC07_18V33_7FF_45C_SPT	7FF	Inline

Summary

The 3.3V Support: Power library provides a full complement of cells to support the assembly of a complete pad ring by abutment. It is supplied as a standard addition to the GPIO libraries and other I/O library offerings from Aragio Solutions that use a compatible pad ring bus structure.

These 7nm libraries are available in inline and staggered flip chip implementations.

The included rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

ESD Protection:

- JEDEC compliant
 - 2KV ESD Human Body Model (HBM)
 - 500 V ESD Charge Device Model (CDM)

Latch-up Immunity:

- JEDEC compliant
 - Tested to I-Test criteria of $\pm 100\text{mA}$ @ 125°C

Cell Size & Form Factor

- Staggered (pad-limited) – $34.08\mu\text{m} \times 214.68\mu\text{m}$
- Inline (core-limited) – $\text{TBD}\mu\text{m} \times \text{TBD}\mu\text{m}$

Recommended operating conditions

Description	Min	Nom	Max	Units
V_{VDD} Core supply voltage	0.675	0.75	0.825	V
	0.765	0.85	0.935	V
	2.97	3.3	3.63	V
V_{DVDD} I/O supply voltage	2.25	2.5	2.75	V
	1.62	1.8	1.98	V
	1.08	1.2	1.32	V
T_{J} Junction temperature	-40	25	125	$^\circ\text{C}$
V_{PAD} Voltage at PAD	$V_{\text{DVSS}} - 0.3$	-	$V_{\text{DVDD}} + 0.3$	V

Characterization Corners *

Model	LPE Type	VDD [1]	DVDD [2]	Temp
FF	Cbest_CCbest	+10%	+10%	-40 $^\circ\text{C}$
FF	Cbest_CCbest	+10%	+10%	125 $^\circ\text{C}$
TT	Ctypical	nominal	nominal	25 $^\circ\text{C}$
TT	Ctypical	nominal	nominal	85 $^\circ\text{C}$
SS	Cworst_CCworst	-10%	-10%	-40 $^\circ\text{C}$
SS	Cworst_CCworst	-10%	-10%	125 $^\circ\text{C}$

[1] VDD = 0.75V & 0.85V

[2] DVDD = 1.2V, 1.8V, 2.5V & 3.3V

* PRELIMINARY

Cell List

Name	Description
Digital Pads *	
STx_IN_001_1833V_NC	Input-only buffer
I/O Power / Ground Pads *	
PWx_VD_RDO_1833V	I/O power (DVDD)
PWx_VS_RDO_1833V	I/O ground (DVSS)
PWx_VS_DRC_1833V	Common ground with I/O ESD
Core Power / Ground Pads *	
PWx_VD_RCD_1033V	Core power (VDD)
PWx_VS_RCD_1033V	Core ground (VSS)
PWx_VS_DRC_1033V	Common ground with Core ESD
Analog Pads *	
ANx_BI_DWR_1833V	1.8V Analog Input cell
ANx_BI_DWR_1033V	0.8V Analog Input cell
Analog Power / Ground Pads *	
PWx_VD_ANA_1033V	Analog power (AVDD) 0.8V
PWx_VS_ANA_1033V	Analog ground (AVSS)
PWx_VD_ANA_1833V	Analog power (ADVDD) 1.8V
PWx_VS_ANA_1833V	Analog ground (ADVSS)
Support Pads	
SPx_CO_000_1833V	Corner cell (rail splitter)
SPx_CO_001_1833V	Corner cell (continuous)
SPx_SP_000_1833V	0.1 μm spacer
SPx_SP_001_1833V	1 μm spacer
SPx_SP_002_1833V	2 μm spacer
SPx_SP_005_1833V	5 μm spacer
SPx_SP_010_1833V	10 μm spacer
SPx_RS_005_1833V	Rail splitter
SPx_RE_SVR_1833V	VREF / HVPS generation
SPx_SP_POC_1833V	POC generation

* Vertical-only (_V) and horizontal only (_H) variants provided
Cell names / descriptions abbreviated

Staggered CUP Cells

CUP_TSMC07_FC	Flip chip with top metal port
CUP_TSMC07_FC_NRV	Flip chip without RV via

Inline CUP Cells

CUP_TSMC07_FC_INLINE	Flip chip with top metal port
CUP_TSMC07_FC_INLINE_NRV	Flip chip without RV via and RDL port

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Published by:

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