

Libraries

Name	Process	Form Factor
RGO_TSMC16_18V33_FFC_20C_I2C	FFC	Staggered CUP
RGO_TSMC12_18V33_FFC_LL_20C_I2C	FFC_LL	Staggered CUP

Summary

The I2C library provides open-drain bi-directional I/O cells designed for the I²C two-line interface. It is compliant with the I²C-bus specification – UMC10204 I²C-bus specification and user manual, Rev.4 – 13 February 2012, NXP.

The design supports the Sm, Fm and Fm+ modes of operation at the I²C bus operating voltage (VDDP) of either extended range 3.3V or standard 1.8V logic.

These libraries are offered at both 16nm and a 12nm shrink. They are available in a staggered CUP wire bond implementation with a flip chip option.

To utilize these cells in the pad ring, an additional library is required – 1.8V Support: Power. That library contains the power cells, the POC cell, and a rail splitter to isolate the I2C cells in their own power domain as recommended. It also contains an input-only buffer, isolated analog I/O, and a full complement of power cells along with corner and spacer cells to assemble a complete pad ring by abutment. The rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

ESD Protection:

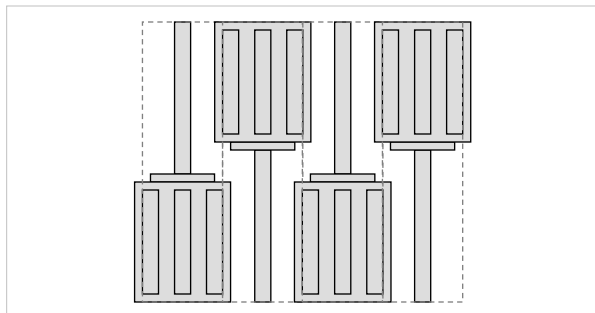
- JEDEC compliant
 - 2KV ESD Human Body Model (HBM)
 - 500 V ESD Charge Device Model (CDM)

Latch-up Immunity:

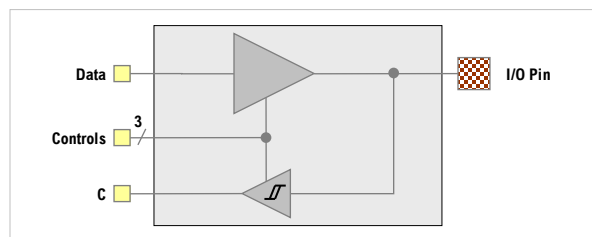
- JEDEC compliant
 - Tested to I-Test criteria of $\pm 100\text{mA}$ @ 125°C

Cell Size & Form Factor

Staggered (pad-limited) – 25.2 μm x 165.024 μm



I2P_ON_003_1833V_NC



Product Features

- Supported I2C operating modes:
 - Standard-mode (Sm) – 100 Kbps data rate
 - Fast mode (Fm) – 400 Kbps data rate
 - Fast mode (Fm+) – 3.4 Mbps data rate
- Open drain operation only (floating NWELL with PMOS used for ESD protection only)
- Built-in output slew rate control to meet I²C T_{of} minimum of (20 x VDDP/5.5V) ns
- Output enable
- Receiver enable
- ESD protection is accomplished with an SCR (no diode to the positive power supply)
- Standard LVCMOS compatible inputs with Schmitt trigger (hysteresis) option
- Power-on sequencing independent design with Power-On Control
- DVDD = 1.62V to 1.98V
- Pad VDDP (power supply reference for Output)
 - 2.7V to 3.63V – extended range 3.3V
 - 1.62V to 1.98V – standard range 1.8V
- The circuit consumes no DC supply current in the static state

An open-drain design, this cell requires an external pull-up resistor to a high voltage power supply. The pull-up power supply (VDDP) can be 3.63V maximum, independent of the I/O cell power supply (DVDD). In a 1.8V I2C bus application, VDDP can track DVDD but it is not necessary. The sizing of the external resistor is application dependent and can range from 1.1 K Ω to 40 K Ω operating at 3.3V.

Vertical-only (_V) and horizontal-only (_H) variants provided.

Recommended operating conditions

Description	Min	Nom	Max	Units	
V _{DVDD} I/O supply voltage	1.62	1.8	1.98	V	
V _{VDDP} External pull-up supply to PAD	3.3V	2.70	3.3	3.63	V
	1.8V	1.62	1.8	1.98	V
V _{VDD} Core supply voltage	0.72	0.8	0.88	V	
T _J Junction temperature	-40	25	125	°C	
V _{PAD} Voltage at PAD	V _{DVSS} - 0.3	-	3.63	V	

Characterization Corners (16nm)

Model	LPE Type	VDD=0.8V	DVDD [1]	Temp
FFGNP	Cbest_CCbest_T	+10%	+10%	-40°C
FFGNP	Cbest_CCbest_T	+10%	+10%	0°C
FFGNP	Cbest_CCbest_T	+10%	+10%	125°C
FFG	Ctypical	+10%	+10%	125°C
TT	Ctypical	nominal	nominal	25°C
TT	Ctypical	nominal	nominal	85°C
SSGNP	Cworst_CCworst_T	-10%	-10%	-40°C
SSGNP	Cworst_CCworst_T	-10%	-10%	0°C
SSGNP	Cworst_CCworst_T	-10%	-10%	125°C

[1] DVDD = 1.8V, 3.0 & 3.3V

Characterization Corners (12nm)

Model	LPE Type	VDD=0.8V	DVDD [1]	Temp
FF	Cbest_CCbest	+10%	+10%	-40°C
FF	Cbest_CCbest	+10%	+10%	0°C
FF	Cbest_CCbest	+10%	+10%	125°C
FFG	Ctypical	+10%	+10%	125°C
TT	Ctypical	nominal	nominal	25°C
TT	Ctypical	nominal	nominal	85°C
SS	Cworst_CCworst	-10%	-10%	-40°C
SS	Cworst_CCworst	-10%	-10%	0°C
SS	Cworst_CCworst	-10%	-10%	125°C

[1] DVDD = 1.8V, 3.0 & 3.3V

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Published by:

Aragio Solutions
2201 K Avenue
Section B Suite 200
Plano, TX 75074-5918
Phone: (972) 516-0999
Fax: (972) 516-0998
Web: <http://www.aragio.com/>

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Printed in the United States of America