

## Libraries

Name	Process	Form Factor
RGO_TSMC16_18V33_FFC_20C_OSC	FFC	Staggered CUP
RGO_TSMC12_18V33_FFC_LL_20C_OSC	FFC_LL	Staggered CUP

## Summary

The 3.3V 100MHz Oscillators library includes a programmable oscillator macro I/O cell.

- 100 MHz programmable oscillator

These libraries are offered at both 16nm and a 12nm shrink. They are available in a staggered CUP wire bond implementation with a flip chip option.

To utilize these cells in the pad ring, an additional library is required – 3.3V Support: Power. That library contains the DVDD/DVSS power cells necessary for ESD protection, the POC and VREF cells, and a rail splitter to isolate the oscillator in its own power domain as recommended. It also contains an input-only buffer, isolated analog I/O, and a full complement of power cells along with corner and spacer cells to assemble a complete pad ring by abutment. The rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

### ESD Protection:

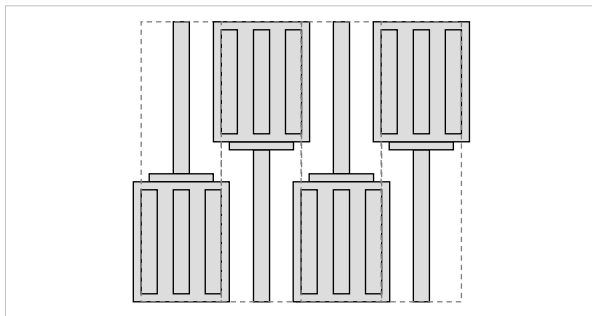
- JEDEC compliant
  - 2KV ESD Human Body Model (HBM)
  - 500 V ESD Charge Device Model (CDM)

### Latch-up Immunity:

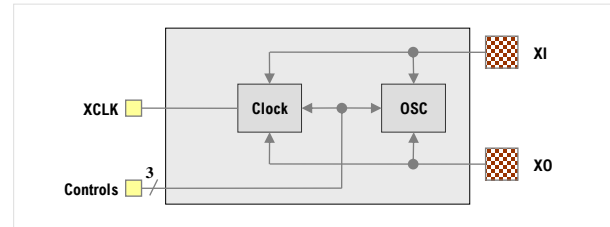
- JEDEC compliant
  - Tested to I-Test criteria of  $\pm 100\text{mA}$  @  $125^\circ\text{C}$

## Cell Size & Form Factor

Staggered (pad-limited) –  $100.8\mu\text{m} \times 165.024\mu\text{m}$



## OSP\_BI\_100\_1833V



## 100 MHz Programmable Oscillator Features

- Programmable drive strength for wider frequency range – 1 MHz to 100 MHz using industry standard external crystals.
- Optimized for stability and minimum jitter
- Power-down mode
- Operates on core power only (VDD/VSS cells embedded)

Vertical-only (\_V) and horizontal-only (\_H) variants provided.

## Recommended operating conditions

Description	Min	Nom	Max	Units
$V_{\text{VDD}}$ Core supply voltage	0.72	0.80	0.88	V
$V_{\text{DVDD}}$ I/O supply voltage	2.97	3.3	3.63	V
	2.25	2.5	2.75	V
	1.62	1.8	1.98	V
$T_{\text{J}}$ Junction temperature	-40	25	125	$^\circ\text{C}$
$V_{\text{PAD}}$ Voltage at XI <sup>[1]</sup>	0	-	$V_{\text{VDD}}$	V

[1] XI can be driven by an external clock for bypass operation. XO should never be driven or loaded by anything other than the oscillator crystal.

## Characterization Corners (16nm)

Model	LPE Type	VDD=0.8V	DVDD [1]	Temp
FFGNP	Cbest_CCbest_T	+10%	+10%	-40°C
FFGNP	Cbest_CCbest_T	+10%	+10%	0°C
FFGNP	Cbest_CCbest_T	+10%	+10%	125°C
FFG	Ctypical	+10%	+10%	125°C
TT	Ctypical	nominal	nominal	25°C
TT	Ctypical	nominal	nominal	85°C
SSGNP	Cworst_CCworst_T	-10%	-10%	-40°C
SSGNP	Cworst_CCworst_T	-10%	-10%	0°C
SSGNP	Cworst_CCworst_T	-10%	-10%	125°C

[1] DVDD = 3.3V, 2.5V, 1.8V & 1.2V.

## Characterization Corners (12nm)

Model	LPE Type	VDD=0.8V	DVDD [1]	Temp
FF	Cbest_CCbest	+10%	+10%	-40°C
FF	Cbest_CCbest	+10%	+10%	0°C
FF	Cbest_CCbest	+10%	+10%	125°C
FFG	Ctypical	+10%	+10%	125°C
TT	Ctypical	nominal	nominal	25°C
TT	Ctypical	nominal	nominal	85°C
SS	Cworst_CCworst	-10%	-10%	-40°C
SS	Cworst_CCworst	-10%	-10%	0°C
SS	Cworst_CCworst	-10%	-10%	125°C

[1] DVDD = 3.3V, 2.5V, 1.8V & 1.2V.

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