GF14: 3.3V GPIO

Libraries

Name	Process	Form Factor	Silicon proven
RGO_GF14_18V33_XM_20C	XM	Staggered	yes
RGO_GF14_18V33_XM_40C	XM	Inline	yes

Summary

A full range of power pads is provided to enable the system designer different options for separate core power (VDD and VSS) and separate I/O padring power and ground (DVDD and DVSS). The ability to isolate separate power domains is also provided. In addition, the I/O library has a full complement of cells that provide the user with the ability to isolate analog I/O's and power within the same padring as the digital I/O's.
Includes:

- Programmable GPIO
- Programmable fault-tolerant GPIO
- Input buffer
- Power supplies
- Isolated analog power supplies
- Oscillators
- Full complement of support pads

ESD Protection

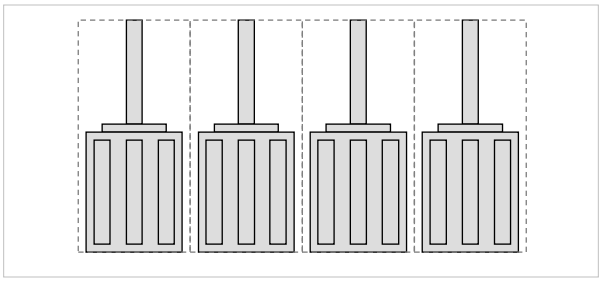
I/O pads are designed with robust ESD protection for all market segments. Passed:

- 2KV ESD Human Body Model (HBM)
- 200 V ESD Machine Model (MM)
- 500 V ESD Charge Device Model (CDM)

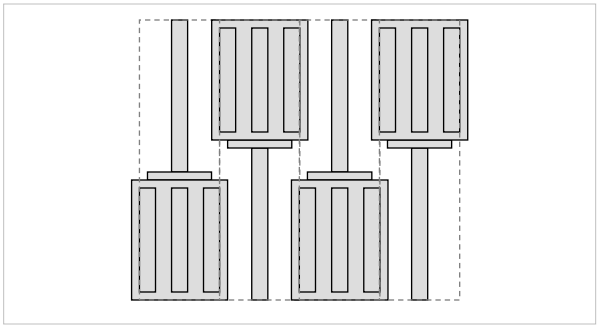
Form factor

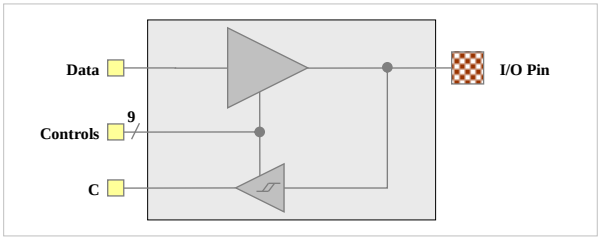
Libraries are offered in both inline (core-limited) and staggered (pad limited) configurations.

Inline (core-limited) – 40µm x 82µm[*]



Staggered (pad-limited) – 25µm x 132µm[*]



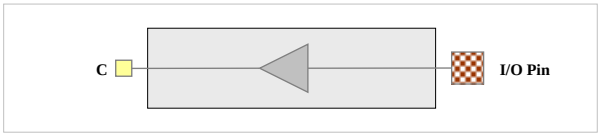


SRx_BI_SDS_33V_STB/ FRx_BI_SDS_33V_STB

Description

SRx_BI_SDS_33V_STB / FRx_BI_SDS_33V_STB are programmable, multi-voltage (1.8V, 3.3V) general purpose, bi-directional I/O buffers with a selectable LVCMOS input or LVCMOS Schmitt trigger input and programmable pull-up / pull-down. In the full-drive mode, this buffer can operate in excess of 100MHz frequency with 15pF external load and 125 MHz with 10pF load, but actual frequency is load and system dependent. A maximum of 175 MHz can be achieved under small capacitive loads.

STx_IN_001_33V_NC



Description

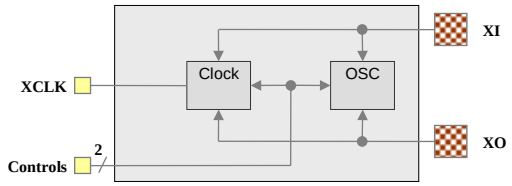
STx_IN_001_33V_NC is an input pad

[*]Pad Sizes

Pad	Width	Height
SRP_BI_SDS_33V_STB	25	132
FRP_BI_SDS_33V_STB	25	140
SRC_BI_SDS_33V_STB	40	82
FRC_BI_SDS_33V_STB	40	92

GF14: 3.3V GPIO

OSx_BI_032_33V



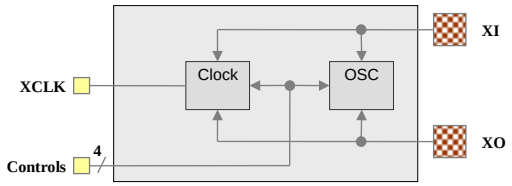
Description

The OSx_BI_032_33V oscillator is designed to generate an asynchronous on-chip clock signal with an appropriate external oscillator crystal. The design has been optimized for low power (1.5 uW typical), stability and minimum jitter using a general purpose 32KHz crystal. The design has been characterized to allow a variation of 4pF to 18pF on each pin.

Key features:

- Very low power (2.6 µW max)
- Bypass mode
- Power down (disable) mode
- Speed-up circuitry for fast startup

OSx_BI_100_33V



Description

The OSx_BI_100_33V oscillator is designed to generate an asynchronous on-chip clock signal with an appropriate external oscillator crystal. The design has been optimized for a wide operating range, stability and minimum jitter using a wide range of industry standard crystals. The design has been characterized to allow a variation of 4pF to 18pF on each pin.

Key features:

- Programmable current for wide frequency range
- Frequency range of 1 MHz to 100 MHz
- DVDD options from 1.5V to 3.3V
- Bypass mode
- Power down (disable) mode

Recommended operating conditions

	Description		Min	Nom	Max	Units
V_{DVDD}	I/O supply voltage		1.62	1.8	1.98	V
			2.97	3.3	3.63	V
T_A	Ambient operating temperature		0	25	100	°C
V_{VDD}	Core supply voltage		0.72	0.8 to 0.9	0.945	V
T_J	Junction temperature		-40	25	125	°C
V_{PAD}	Voltage at PAD		0	-	V_{DVDD}	V
V_{IH}	Input logic high	1.8V	0.65 * V_{DVDD}		V_{DVDD} + 0.3	V
V_{IL}	Input logic low	1.8V	V_{DVSS} - 0.3		0.35 * V_{DVDD}	V
V_{IH}	Input logic high	3.3V	2.0		V_{DVDD} + 0.3	V
V_{IL}	Input logic low	3.3V	V_{DVSS} - 0.3		0.8	V

Characterization Corners

Nominal VDD	Model	VDD	DVDD[1]	Temperature
0.8 – 0.9	FF	+5%	+10%	-40°C
	FF	+5%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C

[1] DVDD = 1.8 and 3.3V

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