GF28: SSTL_15/18 Pad Set

Libraries

Name	Process	CUP	Form Factor
RGO_GF28_18V18_SLP_20C_SSTL_15_18	SLP	yes	staggered
RGO_GF28_18V18_HPP_20C_SSTL_15_18	HPP	yes	staggered

Summary

The SSTL_15/18 pad set is a full complement of I/O, calibration, power, and spacer cells that are necessary to assemble a padring by abutment. Since the SSTL_15/18 normally operates with its own isolated power domain (1.5V/1.8V), a "rail-splitter" support cell (SPP_RS_005_15V) is included to allow the designer to easily break the lines that should not connect to the rest of the padring, while allowing VDD and VSS to be continuous within the padring.

Features

- Full DDR3 capability - 800MHz (1600 Mbps)
- Full DDR2 capability
- Low Power driving standard DDR3 memories
- 1.8V FETs
- Full complement of cells to build padring (20)
- Full ODT Capability - dynamic 6-Bit PVT calibration (external reference resistor)

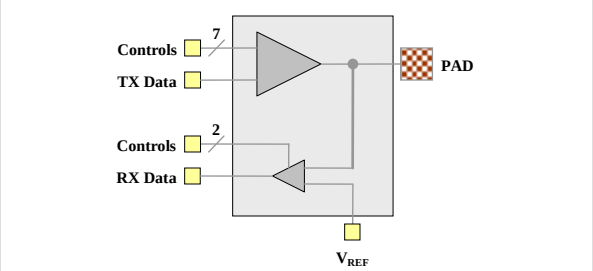
Absolute maximum ratings

Parameter	Description	Value	Units
V_{VDD}	Core supply voltage range	-0.5 to 1.4	V
V_{DVDD}	I/O supply voltage range	-0.5 to 2.1	V
V_{PAD}	Voltage range at PAD	-0.5 to (V_{DVDD} + 0.5)	V

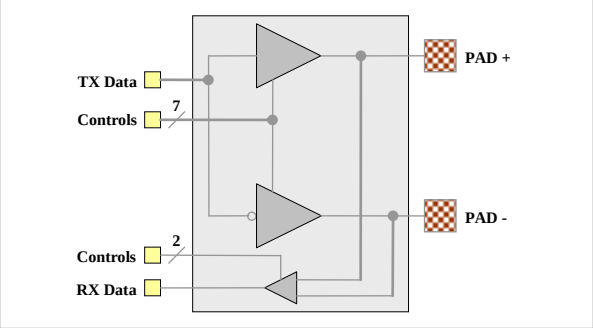
Recommended operating conditions

Parameter	Description	Min	Nom	Max	Units
V_{VDD}	Core supply voltage	0.9	1.0 to 1.1	1.15	V
$V_{DVDD\ (SSTL\_15)}$	I/O supply voltage	1.425	1.5	1.575	V
$V_{DVDD\ (SSTL\_18)}$	I/O supply voltage	1.62	1.8	1.98	V
V_{VREF}	Reference voltage	0.81	0.9	0.99	V
T_A	Ambient operating temperature	0	25	100	°C
T_J	Junction temperature	-40	25	125	°C
V_{PAD}	Voltage at PAD	0		V_{DVDD}	V
$V_{IH\ (dc)}$	DC input logic high	V_{REF} + 0.1		TBD	V
$V_{IL\ (dc)}$	DC input logic low	TBD		V_{REF} - 0.1	V
$V_{IH\ (ac)}$	AC input logic high	V_{REF} + 0.175		-	V
$V_{IL\ (ac)}$	AC input logic low	-		V_{REF} - 0.175	V

SLP_BI_SDS_18V_D – SSTL_15/18 Driver



SLP_CL_SDS_18V_D – SSTL_15/18 Clock Driver



AC Characteristics

Symbol	Parameter		Max	Unit
F	Max frequency		800	MHz
P_{DISS}(TX)	Power dissipation	100 MHz	10.3	mW
		400 MHz	12.7	mW
		800 MHz	15.8	mW

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Characterization Corners

Nominal VDD	Model	VDD	DVDD=1.5V/1.8V	Temperature
1.0-1.1 [1]	FF	+5%	+5%	-40°C
	FF	+5%	+5%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-5%	-40°C
	SS	-10%	-5%	125°C
0.85[2]	FF	+10%	+5%	-40°C
	FF	+10%	+5%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-5%	-40°C
	SS	-10%	-5%	125°C

[1] SLP process only
[2] HPP process only

Physical size

Name	Width	Height	Units
SLP_BI_SDS_18V_D/DVDD/DVSS/PDO	40	205	µm
SLP_CL_SDS_18V_D_PWR	80	205	µm
SLP_SP_CAL_SDS_18V	20	205	µm
SLP_RE_000_1518V	20	205	µm
PVP_VD_RCD_1018V	20	205	µm
PVP_VS_RCD_1018V	20	205	µm
SVP_SP_000_1518V	0.1	205	µm
SVP_SP_001_1518V	1	205	µm
SVP_SP_005_1518V	5	205	µm
SVP_SP_020_1518V	20	205	µm
SPP_RS_005_1518V	5	205	µm
SPP_AD_SSTL_1518V	20	205	µm
SVP_CO_001_15V	205	205	µm

Cell summary

Name	Description
SLP_BI_SDS_18V_D /DVDD/DVSS/PDO	SSTL_15/18 I/O pad with power
SLP_CL_SDS_18V_D_PWR	Differential clock buffer with DVDD/DVSS
SLP_SP_CAL_SDS_18V	Calibration pad
SLP_RE_000_1518V	V_{REF} pad
PVP_VD_RCD_1018V	Core V_{DD} with VREF bus
PVP_VS_RCD_1018V	Core V_{SS} pad with VREF bus
SVP_SP_000_1518V	0.1 µm spacer
SVP_SP_001_1518V	1 µm spacer
SVP_SP_005_1518V	5 µm spacer
SVP_SP_020_1518V	20 µm spacer
SPP_RS_005_1518V	DVDD, DVSS, POC, CP[1..3], CN[1..3] and VREF rail splitter
SPP_AD_SSTL_1518V	Adapter to staggered libraries
SVP_CO_001_1518V	Corner cell

Published by:

Aragio Solutions
2201 K Avenue
Section B Suite 200
Plano, TX 75074-5918
Phone: **(972) 516-0999**
Fax: **(972) 516-0998**
Web: http://www.aragio.com/