GF28: subLVDS Pad Set

Libraries

Name	Process	CUP	Form Factor
RGO_GF28_18V18_SLP_UC_SUBLVDS	SLP	yes	staggered
RGO_GF28_18V18_HPP_UC_SUBLVDS	HPP	yes	staggered

Summary

The LVDS I/O is a three-module design (input, output and reference block). The LSP_OU_800_18V_T is a 1GHz (2GBit/s) LVDS Driver, LDP_IN_800_18V_DN is a 1GHz (2GBit/s) LVDS Receiver and the LDP_RE_009_18V is the voltage reference and current bias for up to 16 drivers. The LSP_OU_800_18V_T is designed to drive either 50Ω or 100Ω differential termination. This cell has been designed to meet the standard SubLVDS specifications (SMIA 1.0 Part 2:CCP2).

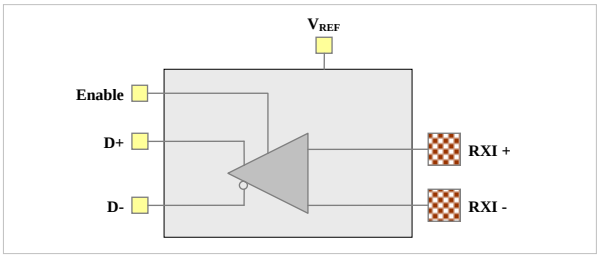
Absolute maximum ratings

Symbol	Description	Value	Units
V_{VDD}	Core supply voltage range	-0.5 to 1.2	V
V_{DVDD}	I/O supply voltage range	-0.5 to 2.95	V
V_{PAD}	Voltage range at PAD	-0.5 to (V_{DVDD} + 0.5)	V
T_J	Junction operating temperature range	-55 to 150	°C

Recommended operating conditions

Symbol	Description	Min	Nom	Max	Units
V_{VDD}	Core supply voltage	0.9	1.0 to 1.1	1.115	V
V_{DVDD}	I/O supply voltage	1.62	1.80	1.98	V
V_{VREF}	Reference voltage		0.9		V
T_A	Ambient operating temperature	0	25	100	°C
T_J	Junction temperature	-40	25	125	°C
V_{PAD}	Voltage at PAD	-0.3V		V_{DVDD}+0.3V	V

LDP_IN_800_18V_DN: 1GHz SubLVDS Input



Key features:

- Powered from 1.8V ±10% and 1.0V(±10%) to 1.1V(-10%/+5%) core power supplies
- Operates up to 1GHz (2Gbps)
- Input receive sensitivity of 50mV peak differential (without hysteresis)
- Common mode range from 0.4V to 1.4V (limited by Power Supply)
- Power-up Sequence Independent
- Duty Cycle Distortion (DCD) less than 50ps
- Power consumption is 1.7 mW typical and 4.7 mW maximum

AC Characteristics

Parameter	Typ	Max	Units	Conditions
Propagation Delay	0.5	0.8	ns	
Input duty cycle distortion	50		ps	Minimum input swing, 100mV common mode noise from 50MHz to 1GHz
DVDD Power Supply Sensitivity	2		ps/mV	DVDD from -10% to -15% over all PVT, minimum input differential
VDD Power Supply Sensitivity	2		ps/mV	VDD from -10% to -15% over all PVT, minimum input differential
Maximum Operating Frequency	1.0		GHz	All noise, jitter, and tdcd measured at 1GHz
Maximum Data Rate	2.0		Gb/s	
Power consumption	1.7	4.7	mW	

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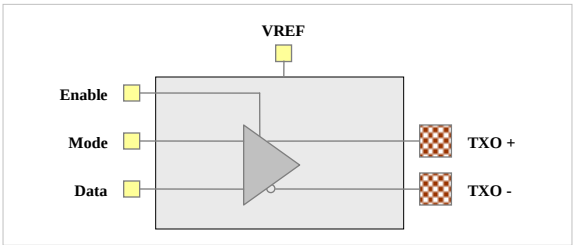
LSP_OU_800_18V_T: 1GHz subLVDS Output Pad



Key features:

- Powered from 1.8V ±10% and 1.0V to 1.1V (±10%) core power supplies
- Operates up to 1.0GHz (2.0 Gbps) with external 1pF load
- Common mode output range 0.90 Volts +/-50mV
- Power-up Sequence Independent
- Differential Skew between TXO_P and TXO_N 50ps
- Mode control for output drive control to drive either 100Ω (1.5 mA typical) or 50Ω (3 mA typical) termination
- Power consumption at 1GHz is 8.5 mW typical and 15.2 mW maximum

AC Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
t_{PHL}	Differential high to low propagation delay	R_L = 100 Ω C_L = 1 pF		480	710	ps
t_{PLH}	Differential low to high propagation delay	R_L = 100 Ω C_L = 1 pF		480	710	ps
t_{skew1}	Differential skew between t_{PHL} and t_{PLH}			50[1]		ps
t_{skew2}	Channel-to-channel skew			100		ps
t_{rise}	V_{OD} differential rise time	20% to 80%	120		250	ps
t_{fall}	V_{OD} differential fall time	20% to 80%	120		250	ps

[1] The maximum differential skew (t_{skew1}) must be at least 100 pSec less than the actual Differential rise or fall times (t_{rise} or t_{fall}) at any specified valid operating condition.

Characterization Corners

Nominal VDD	Model	VDD	DVDD = 1.8V	Temperature
1.0-1.1 [1]	FF	+5%	+10%	-40°C
	FF	+5%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
0.85[2]	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C

[1] SLP process only
[2] HPP process only

Cell summary

Name	Description
LDP_IN_800_18V_DN	1GHz SubLVDS input cell
LSP_OU_800_18V_T	1GHz SubLVDS output cell
LDP_RE_009_18V	V_{REF} pad
PVP_VD_RCD_10V	Core power pad with VREF
PVP_VS_RCD_10V	Power pad for VSS with VREF bus
PVP_VD_PDO_18V	Driver power pad with POC control
PVP_VD_RDO_18V	Driver power pad
PVP_VS_RDO_18V	I/O ground supply with VREF bus
SVP_SP_001_18V	0.1 µm spacer
SVP_SP_001_18V	1 µm spacer
SVP_SP_005_18V	5 µm spacer
SVP_SP_010_18V	10 µm spacer
SPP_RS_005_18V	DVDD, DVSS, POC, BIAS and VREF rail splitter
SPC_SPC_AD_UN	Core limited library adapter pad

Physical sizes

Pad name	Width	Height[*]	Units
LDP_RE_009_18V	40	139	µm
LDP_IN_800_18V_DN	40	117	µm
LSP_OU_800_18V_T	50	129	µm
PVP_VD_RCD_12V	20	117	µm
PVP_VS_RCD_12V	20	117	µm
PVP_VD_PDO_18V	20	117	µm
PVP_VD_RDO_18V	20	117	µm
PVP_VS_RDO_18V	20	117	µm
SVP_SP_000_18V	0.1	117	µm
SVP_SP_001_18V	1	117	µm
SVP_SP_005_18V	5	117	µm
SVP_SP_010_18V	10	117	µm
SPP_RS_005_18V	5	117	µm
SPP_SPC_AD_UN	20	117	µm

[*] Includes CUP bond opening.

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