

Libraries

Name	Process	Form Factor	Silicon proven
RGO_GF28_18V25_SLP_20C	SLP	staggered	yes
RGO_GF28_18V25_SLP_40C	SLP	Inline	yes
RGO_GF28_18V25_HPP_20C	HPP	staggered	4Q11
RGO_GF28_18V25_HPP_40C	HPP	Inline	4Q11

Summary

A full range of power pads is provided to enable the system designer different options for separate core power (VDD and VSS) and separate I/O padding power and ground (DVDD and DVSS). The ability to isolate separate power domains is also provided. In addition, the I/O library has a full complement of cells that provide the user with the ability to isolate analog I/O's and power within the same padding as the digital I/O's.

Includes:

- Programmable GPIO
- Programmable fault-tolerant GPIO
- Input buffer
- Power supplies
- Isolated analog power supplies
- Oscillators
- Full complement of support pads

ESD Protection

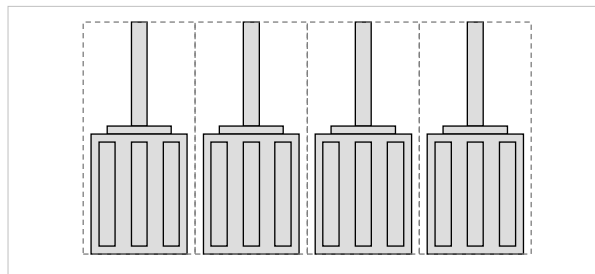
I/O pads are designed with robust ESD protection for all market segments. Passed:

- 2KV ESD Human Body Model (HBM)
- 200 V ESD Machine Model (MM)
- 500 V ESD Charge Device Model (CDM)

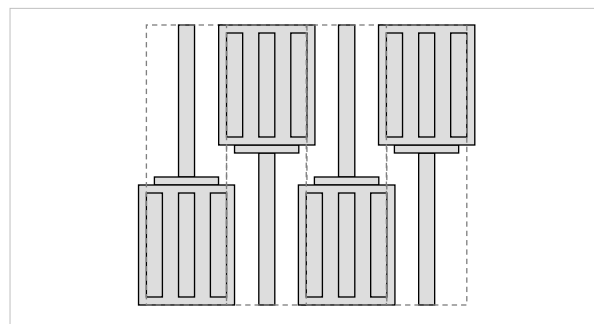
Form factor

Libraries are offered in both inline (core-limited) and staggered (pad limited) configurations.

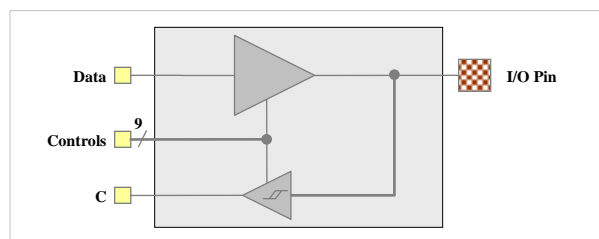
Inline (core-limited) – 40µm x 58µm^[*]



Staggered (pad-limited) – 20µm x 117µm^[*]



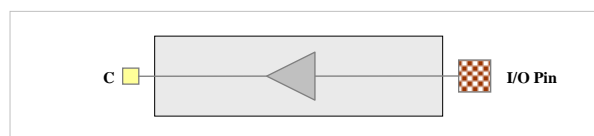
SRx_BI_SDS_25V_STB/ FRx_BI_SDS_25V_STB



Description

SRx_BI_SDS_25V_STB / FRx_BI_SDS_25V_STB are programmable, multi-voltage (1.5V, 1.8V, 2.5V) general purpose, bi-directional I/O buffers with a selectable LVCMOS input or LVCMOS Schmitt trigger input and programmable pull-up / pull-down. In the full-drive mode, this buffer can operate in excess of 100MHz frequency with 15pF external load and 125 MHz with 10pF load, but actual frequency is load and system dependent. A maximum of 200 MHz can be achieved under small capacitive loads.

STx_IN_001_25V_NC



Description

STx_IN_001_25V_NC is an input pad

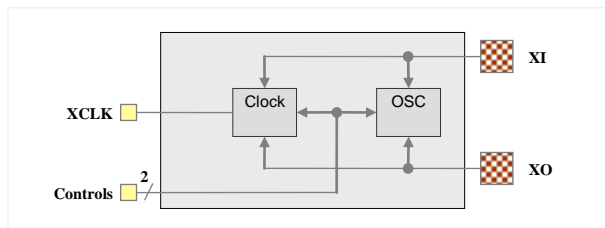
[*]Pad Sizes

Pad	Width	Height
SRP_BI_SDS_25V_STB	25	128
FRP_BI_SDS_25V_STB	25	140
SRC_BI_SDS_25V_STB	40	82
FRC_BI_SDS_25V_STB	40	92

GF28: 2.5V GPIO



OSx_BI_032_25V



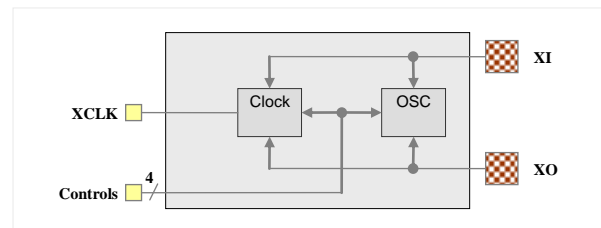
Description

The OSx_BI_032_25V oscillator is designed to generate an asynchronous on-chip clock signal with an appropriate external oscillator crystal. The design has been optimized for low power (1.5 uW typical), stability and minimum jitter using a general purpose 32KHz crystal. The design has been characterized to allow a variation of 4pF to 18pF on each pin.

Key features:

- Very low power (2.6 μW max)
- Bypass mode
- Power down (disable) mode
- Speed-up circuitry for fast startup

OSx_BI_100_25V



Description

The OSx_BI_100_25V oscillator is designed to generate an asynchronous on-chip clock signal with an appropriate external oscillator crystal. The design has been optimized for a wide operating range, stability and minimum jitter using a wide range of industry standard crystals. The design has been characterized to allow a variation of 4pF to 18pF on each pin.

Key features:

- Programmable current for wide frequency range
- Frequency range of 1 MHz to 100 MHz
- DVDD options from 1.5V to 2.5V
- Bypass mode
- Power down (disable) mode

Recommended operating conditions

Description	Min	Nom	Max	Units
V _{DVDD} I/O supply voltage	1.35	1.5	1.65	V
	1.62	1.8	1.98	V
	2.25	2.5	2.75	V
T _A Ambient operating temperature	0	25	100	°C
V _{VDD} Core supply voltage	0.9	1.0 to 1.1	1.155	V
T _J Junction temperature	-40	25	125	°C
V _{PAD} Voltage at PAD	0	-	V _{DVDD}	V
V _{IH} Input logic high	0.7 * V _{DVDD}		V _{DVDD} + 0.3	V
V _{IL} Input logic low	V _{DVSS} - 0.3		0.3 * V _{DVDD}	V

Characterization Corners

Nominal VDD	Model	VDD	DVDD ^[1]	Temperature
1.0-1.1 (SLP)	FF	+5%	+10%	-40°C
	FF	+5%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
0.85 (HPP)	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C

^[1] DVDD = 1.5, 1.8 and 2.5V

© 2006-2011 Aragio Solutions. All rights reserved.

Information in this document is subject to change without notice. Aragio Solutions may have patents, patent applications, trademarks, copyrights or other intellectual property rights covering subject matter in this document. Except as expressly provided in any written license agreement from Aragio, the furnishing of this document does not give you any license to the patents, trademarks, copyrights, or other intellectual property.

Published by:

Aragio Solutions
 2201 K Avenue
 Section B Suite 200
 Plano, TX 75074-5918
Phone: (972) 516-0999
Fax: (972) 516-0998
Web: <http://www.aragio.com/>

While every precaution has been taken in the preparation of this book, the publisher assumes no responsibility for errors or omissions, or for damages resulting from the use of the information contained herein. This document may be reproduced and distributed in whole, in any medium, physical or electronic, under the terms of a license or nondisclosure agreement with Aragio.

Printed in the United States of America