

GF28: LVDS Pad Set



Libraries

Name	Process	CUP	Form Factor
RGO_GF28_18V25_SLP_UC_LVDS	SLP	yes	staggered
RGO_GF28_18V25_HPP_UC_LVDS	HPP	yes	staggered

Summary

The LVDS I/O is a three-module design (input, output and reference block). The LDP_OU_800_18V_T is a 2Gbit/s LVDS Driver, LDP_IN_800_25V_DN is a 2.4Gbit/s LVDS Receiver and the LDP_RE_000_18V is the voltage reference for up to 16 drivers. The LDP_OU_800_18V_T is designed to drive either 50Ω or 100Ω differential termination. This cell has been designed to meet a set of the standard LVDS specifications (IEEE Std 1596.3-1996, Low Voltage Differential Signaling).

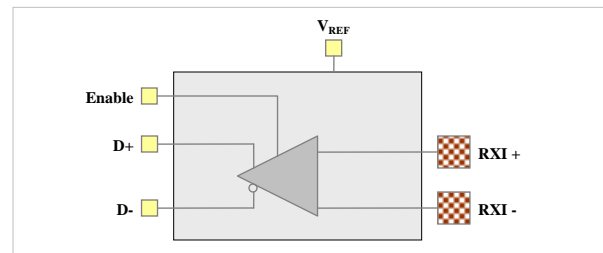
Absolute maximum ratings

Symbol	Description	Value	Units
V _{VDD}	Core supply voltage range	-0.5 to 1.2	V
V _{DVDD}	I/O supply voltage range	-0.5 to 2.95	V
V _{PAD}	Voltage range at PAD	-0.5 to (V _{DVDD} + 0.5)	V
T _J	Junction operating temperature range	-55 to 150	°C

Recommended operating conditions

Symbol	Description	Min	Nom	Max	Units
V _{VDD}	Core supply voltage	0.9	1.0 to 1.1	1.115	V
V _{DVDD}	I/O supply voltage	1.62	1.8	1.98	V
V _{VREF}	Reference voltage		1.2		V
T _A	Ambient operating temperature	0	25	100	°C
T _J	Junction temperature	-40	25	125	°C
V _{PAD}	Voltage at PAD	-0.3V		V _{DVDD} +0.3V	V

LDP_IN_800_25V_DN: 1.2GHz LVDS Input



Key features:

- Powered from 1.8V ±10% and 1.0V (±10%) to 1.1V (-10%/+5%) core power supplies
- Operates up to 1.2GHz (2.4Gbps)
- Input receive sensitivity of 75mV peak differential (without hysteresis)
- Common mode range from 0V to 2.4V (limited by Power Supply)
- Power-up sequence independent
- Power consumption is 1.8 mW typical and 5 mW maximum

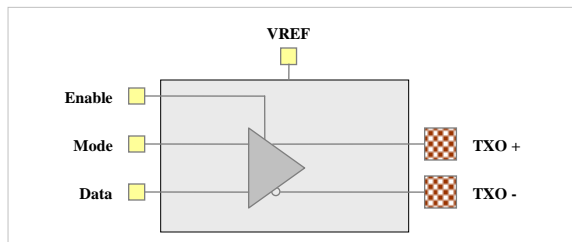
AC Characteristics

Parameter	Typ	Max	Units	Conditions
Propagation delay	0.5	0.8	ns	The slew rate for propagation delays, duty cycle distortion and maximum operating frequency are 1V/ns
Maximum operating frequency	1.2		GHz	All noise, jitter, and t _{dcd} measured at 1.2GHz
Maximum data rate	2.4		Gb/s	

GF28: LVDS Pad Set



LDP_OU_800_18V_T: 1GHz LVDS Output Pad



Key features:

- Powered from 1.8V $\pm 10\%$ and 1.0V to 1.1V ($\pm 10\%$) core power supplies
- Operates up to 1 GHz (2Gbps) with external 1 pF load
- Common mode output range 1.22 Volts $\pm 50\text{mV}$
- Power-up Sequence Independent
- Differential Skew between TXO_P and TXO_N 40ps
- Mode control for output drive control to drive either 100 Ω (3.25 mA) or 50 Ω (6.50 mA) termination
- Power consumption at 1 GHz is 11.4 mW typical and 15 mW maximum

AC Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
t _{PHL}	Differential high to low propagation delay	R _L = 100 Ω C _L = 1 pF	480	710		ps
t _{PLH}	Differential low to high propagation delay	R _L = 100 Ω C _L = 1 pF	480	710		ps
t _{rise}	V _{OD} differential rise time	20% to 80%	120	250		ps
t _{fall}	V _{OD} differential fall time	20% to 80%	120	250		ps

Characterization Corners

Nominal VDD	Model	VDD	DVDD = 1.8V	Temperature
1.1 ^[1]	FF	+5%	+10%	-40°C
	FF	+5%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
1.0 ^[1]	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
0.85 ^[2]	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C

^[1] SLP process only
^[2] HPP process only

Cell summary

Name	Description
LDP_IN_800_25V_DN	1.2 GHz LVDS input cell
LDP_OU_800_18V_T	1 GHz LVDS output cell
LDP_RE_000_18V	V _{REF} pad
PVP_VD_RCD_10V	Core power pad with VREF
PVP_VS_RCD_10V	Power pad for VSS with VREF bus
PVP_VD_PDO_18V	Driver power pad with POC control
PVP_VD_RDO_18V	Driver power pad
PVP_VS_RDO_18V	I/O ground supply with VREF bus
SVP_SP_001_18V	0.1 μm spacer
SVP_SP_001_18V	1 μm spacer
SVP_SP_005_18V	5 μm spacer
SVP_SP_010_18V	10 μm spacer
SPP_RS_005_18V	DVDD, DVSS, POC, BIAS and VREF rail splitter
SPC_SPC_AD_UN	Core limited library adapter pad

Physical sizes

Pad name	Width	Height ^[*]	Units
LDP_RE_000_18V	40	134	μm
LDP_IN_800_25V_DN	40	117	μm
LDP_OU_800_18V_T	50	129	μm
PVP_VD_RCD_10V	20	117	μm
PVP_VS_RCD_10V	20	117	μm
PVP_VD_PDO_18V	20	117	μm
PVP_VD_RDO_18V	20	117	μm
PVP_VS_RDO_18V	20	117	μm
SVP_SP_000_18V	0.1	117	μm
SVP_SP_001_18V	1	117	μm
SVP_SP_005_18V	5	117	μm
SVP_SP_010_18V	10	117	μm
SPP_RS_005_18V	5	117	μm
SPP_SPC_AD_UN	20	117	μm

[*] Includes CUP bond opening.

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Aragio Solutions
2201 K Avenue
Section B Suite 200
Plano, TX 75074-5918
Phone: (972) 516-0999
Fax: (972) 516-0998
Web: <http://www.aragio.com/>

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