

## Libraries

Name	Process	Form Factor	Silicon proven
RGO_GF28_18V33_SLP_20C_RF	SLP	staggered	yes
RGO_GF28_18V33_HPP_20C_RF	HPP	staggered	yes

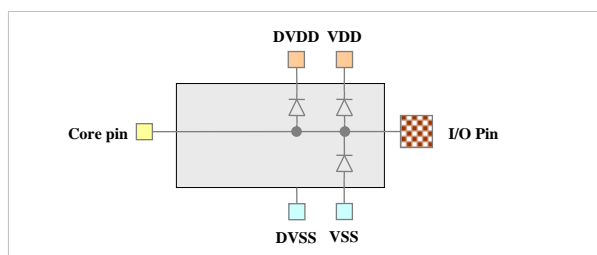
## Includes

- Analog / RF cells
  - Low voltage LNA input pad (1.5V)
  - High voltage LNA input pad (3.3V)
  - PA output pad, 5V tolerant
  - 10GHz analog (thick gate) signal pad with multiple input resistance options, 5V tolerant
- Discrete ESD protection components
  - RF diodes
  - SCR's

## Analog / RF Pads

### ANP\_IN\_LAN\_10V

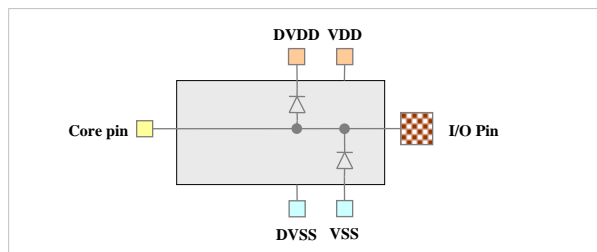
ANP\_IN\_LNA\_10V is a 0 to 1.5V analog I/O pad optimized for low capacitance. This is designed to protect thin gate oxide input devices. The layout uses wide metal 3 interconnect (14  $\mu\text{m}$ ) for low inductance from the bond pad to the core.



Pin capacitance: 790 fF (SLP process), 843 fF (HPP process)

### ANP\_IN\_LNA\_33V

ANP\_IN\_LNA\_33V is a 0 to 3.3V analog I/O pad optimized for low capacitance. The layout uses wide metal 3 interconnect (12  $\mu\text{m}$ ) for low inductance from the bond pad to the core.



Pin capacitance: 660 fF (SLP process), 673 fF (HPP process)

## ESD Protection

I/O pads are designed with robust ESD protection for all market segments. Passed:

- 2KV ESD Human Body Model (HBM)
- 200 V ESD Machine Model (MM)
- 500 V ESD Charge Device Model (CDM)

## RF Diodes

The set of PPLUS\_NWELL\_DIODE\_x RF diodes are selected to provide minimum capacitance for RF applications and high current handling capability for good ESD protection.

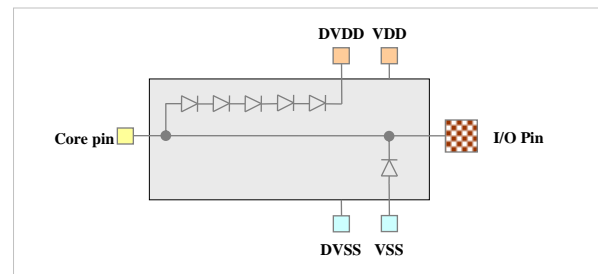
## Silicon-Controlled Rectifiers (SCR)

The set of P+ to Nwell SCR discrete components are selected to provide the lowest capacitance with the highest ESD protection. These components have been used in I/O pads to demonstrate over 6KV ESD protection.

### ANP\_OU\_PWA\_5T

ANP\_OU\_PWA\_5T is an analog I/O pad optimized for low capacitance which uses SCRs for ESD clamp devices.

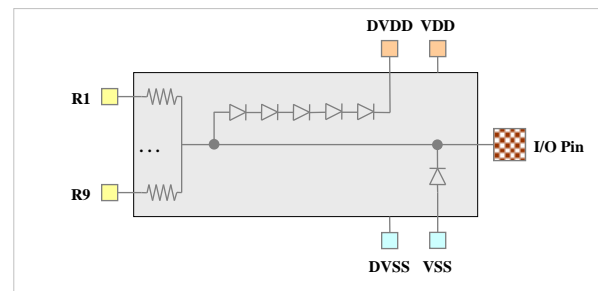
The stacked diode ESD structure from DVDD to the I/O pin provides extended overvoltage protection. With a 3.3V power supply, this I/O pad is 5V tolerant. Dropping to an I/O domain power supply of 1.8V, the pad is 3.3V tolerant.



Pin capacitance: 692 fF (SLP process), 702 fF (HPP process)

### ANP\_BI\_DWR\_5T

ANP\_BI\_DWR\_5T is a bi-directional analog signal pad with selectable input resistance. Resistors R1 to R4 and R6 to R9 can be used in parallel to achieve the desired resistance value as low as 1.3 ohms.



This structure can then be used with output amplifiers for which R5 can be used in the feedback path. If used in this manner, R1 to R4 and R6 to R9 should be individually connected to isolated fingers of the driver transistors.

## Recommended operating conditions

Description	Min	Nom	Max	Units
V <sub>DVDD</sub> I/O supply voltage	2.70	3.3	3.63	V
T <sub>A</sub> Ambient operating temperature	0	25	100	°C
V <sub>VDD</sub> Core supply voltage	0.9	1.0-1.1	1.15	V
T <sub>J</sub> Junction temperature	-40	25	125	°C
V <sub>PAD</sub> Voltage at PAD	V <sub>DVSS</sub> - 0.3	-	V <sub>VDDP</sub>	V

## Characterization Corners

Nominal VDD	Model	VDD	DVDD = 3.0/3.3V	Temperature
1.1 <sup>[1]</sup>	FF	+5%	+10%	-40°C
	FF	+5%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
1.0 <sup>[1]</sup>	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
0.85 <sup>[2]</sup>	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C

<sup>[1]</sup> SLP process only

<sup>[2]</sup> HPP process only

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