

Libraries

Name	Process	Form Factor
RGO_GF28_18V15_SLP_25C_LPDDR3_DDR4	SLP	Staggered
RGO_GF28_18V15_HPP_25C_LPDDR3_DDR4	HPP	Staggered

Summary

The LPDDR2/3_DDR3/4 libraries contain the 6-way combo driver/receiver cells with embedded power cells, the driver impedance calibration cell, and the DDR voltage reference cell providing both single-ended and differential signaling for LPDDR2, LPDDR3, DDR3, DDR3L, DDR3U, and DDR4 applications. Also included is a full complement of power, corner and spacer cells to assemble a complete pad ring by abutment. An included rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

Full DDR4 capability

- Data rates – 1600 MT/s, 1866 MT/s, 2133 MT/s, 2400 MT/s

Full DDR3 / DDR3L / DDR3U capability

- Data rates – 800 MT/s, 1066 MT/s, 1333 MT/s, 1600 MT/s, 1866 MT/s, 2133 MT/s

Full LPDDR3 capability

- Data rates – 1333 MT/sec, 1600 MT/sec

Full LPDDR2 capability

- Data rates – 466 MT/sec, 1066 MT/sec

ESD Protection:

- JEDEC compliant
 - 2KV ESD Human Body Model (HBM)
 - 200 V ESD Machine Model (MM)
 - 500 V ESD Charge Device Model (CDM)

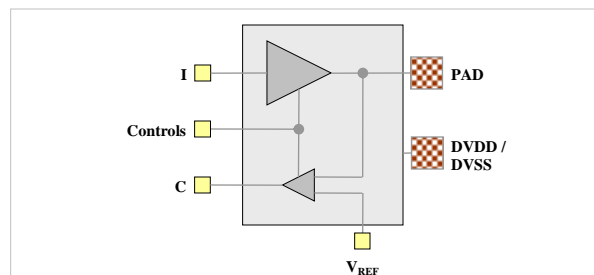
Latch-up Immunity:

- JEDEC compliant
 - Tested to I-Test criteria of $\pm 100\text{mA}$ @ 125°C

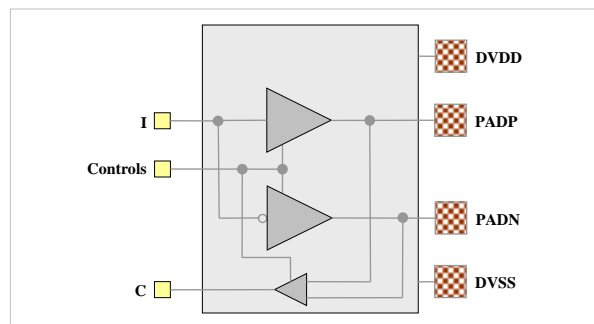
Recommended operating conditions

Parameter	Description	Min	Nom	Max	Units	
V_{VDD}	Core supply voltage	SLP	0.90	1.00	1.10	V
			0.99	1.10	1.155	V
		HPP	0.765	0.85	0.935	V
			0.81	0.90	0.945	V
V_{DVDD}	I/O supply voltage	DDR4	1.14	1.2	1.26	V
		DDR3	1.425	1.5	1.575	V
		DDR3L	1.283	1.35	1.45	V
		DDR3U	1.19	1.25	1.31	V
		LPDDR2	1.14	1.2	1.3	V
		LPDDR3	1.14	1.2	1.3	V
T_J	Junction temperature	-40	25	+125	°C	
V_{PAD}	Voltage at PAD	V_{DVSS}		V_{DVDD}	V	

SLP_BI_SDS_1215V_D_x: Single-Ended Driver



SLP_CL_SDS_1215V_D_PWR : Differential Driver



Product Features

- User programmable drive strength
 - DDR3 – $Z_{OUT} = 34 / 40 \Omega$
 - DDR4 – $Z_{OUT} = 34 / 48 \Omega$
 - LPDDR2 – $Z_{OUT} = 34 / 40 / 48 / 60 / 80 \Omega$
 - LPDDR3 – $Z_{OUT} = 34 / 40 \Omega$
- User programmable on-die termination
 - DDR3 – 120 / 60 / 40 / 30 / 24 / 20 / 17 Ω
 - DDR4 – 240 / 120 / 80 / 60 / 48 / 40 / 34 Ω
 - LPDDR3 – 240 / 120 / 80 / 60 / 48 / 40 / 34 Ω
- Operating frequency up to 1200 MHz (2400 MT/sec) data rate)

GF28: LPDDR2/3_DDR3/4



Cell summary

Name	Description
SLP_BI_SDS_1215V_D_DVDD/DVSS/PDO	Bi-directional driver / receiver cell with power
SLP_CL_SDS_1215V_D_PWR	Differential clock driver / receiver with DVDD / DVSS
SLP_SP_CAL_SDS_1215V	DDR3 / DDR4 calibration pad
SLP_SP_CSH_0915V	Calibration code bus driver
SLP_RE_000_1215V	DDR3 / DDR4 voltage reference
PVP_VD_RCD_0915V	Core power (VDD)
PVP_VS_RCD_0915V	Core ground (VSS)
SVP_SP_000_1215V	0.1 μ m spacer
SVP_SP_001_1215V	1 μ m spacer
SVP_SP_005_1215V	5 μ m spacer
SVP_SP_020_1215V	20 μ m spacer
SVP_CO_001_1215V	Corner cell
SPP_RS_005_1215V	Rail splitter
SPP_AD_SSTL_1215V	DDR to staggered 1.8V GPIO adapter
SPP_SP_CAP_1215V	DVDD/DVSS decoupling cap

Physical size

Name	Width	Height	Units
SLP_BI_SDS_1215V_D_DVDD/DVSS/PDO	50	205	μ m
SLP_CL_SDS_1215V_D_PWR	100	205	μ m
SLP_SP_CAL_SDS_1215V	40	205	μ m
SLP_SP_CSH_0915V	20	205	μ m
SLP_RE_000_1215V	40	205	μ m
PVP_VD_RCD_0915V	25	205	μ m
PVP_VS_RCD_0915V	25	205	μ m
SVP_SP_000_1215V	0.1	205	μ m
SVP_SP_001_1215V	1	205	μ m
SVP_SP_005_1215V	5	205	μ m
SVP_SP_020_1215V	20	205	μ m
SVP_CO_001_1215V	205	205	μ m
SPP_RS_005_1215V	5	205	μ m
SPP_AD_SSTL_1215V	20	205	μ m
SPP_SP_CAP_1215V	10	10	μ m

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