

# GF40: SSTL\_15 Pad Set



## Libraries

Name	Process	CUP	Form Factor
RGO_GF40_25V15_LP_30C_SSTL_15	LP	yes	staggered

## Summary

The SSTL\_15 pad set is a full complement of I/O, calibration, power, and spacer cells that are necessary to assemble a padding by abutment. Since the SSTL\_15 normally operates with its own isolated power domain (1.5V), a “rail-splitter” support cell (SPP\_RS\_005\_15V) is included to allow the designer to easily break the lines that should not connect to the rest of the padding, while allowing VDD and VSS to be continuous within the padding.

## Features

- Full DDR3 capability - 800MHz (1600 Mbps)
- Low Power driving standard DDR3 memories
- 2.5V FETs
- Full complement of cells to build padding (20)
- Full ODT Capability:
  - Either fixed 6-Bit programming (program from core)
  - Or, dynamic 6-Bit PVT calibration (external reference resistor)

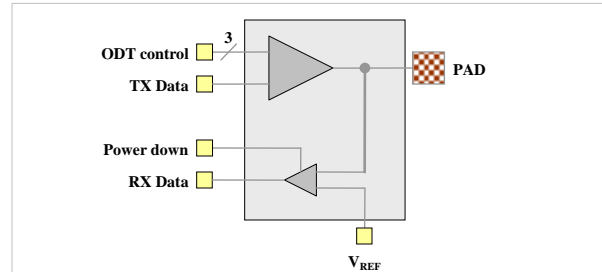
## Absolute maximum ratings

Parameter	Description	Value	Units
V <sub>VDD</sub>	Core supply voltage range	-0.5 to 1.4	V
V <sub>DVDD</sub>	I/O supply voltage range	-0.5 to 2.1	V
V <sub>PAD</sub>	Voltage range at PAD	-0.5 to (V <sub>DVDD</sub> + 0.5)	V

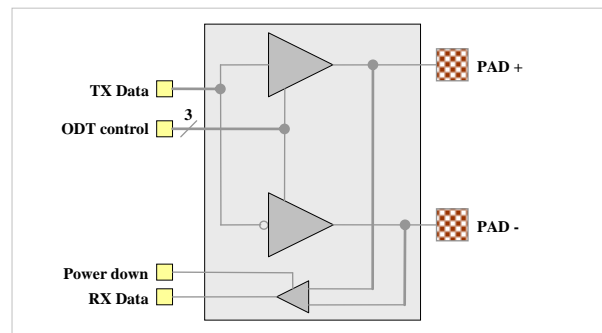
## Recommended operating conditions

Parameter	Description	Min	Nom	Max	Units
V <sub>VDD</sub>	Core supply voltage	0.99	1.1 to 1.2	1.26	V
V <sub>DVDD</sub>	I/O supply voltage	1.425	1.5	1.575	V
V <sub>VREF</sub>	Reference voltage	0.67	0.75	0.8	V
T <sub>A</sub>	Ambient operating temperature	0	25	100	°C
T <sub>J</sub>	Junction temperature	-40	25	125	°C
V <sub>PAD</sub>	Voltage at PAD	0		V <sub>DVDD</sub>	V
V <sub>IH (dc)</sub>	DC input logic high	V <sub>REF</sub> + 0.1		TBD	V
V <sub>IL (dc)</sub>	DC input logic low	TBD		V <sub>REF</sub> - 0.1	V
V <sub>IH (ac)</sub>	AC input logic high	V <sub>REF</sub> + 0.175		-	V
V <sub>IL (ac)</sub>	AC input logic low	-		V <sub>REF</sub> - 0.175	V

## SLP\_BI\_SDS\_15V\_D – SSTL\_15 Driver



## SLP\_CL\_SDS\_15V\_D – SSTL\_15 Clock Driver



## AC Characteristics

Symbol	Parameter	Max	Unit
F	Max frequency	800	MHz
		100 MHz	11.2 mW
P <sub>DISS</sub>	Power dissipation	400 MHz	14.4 mW
		800 MHz	16.0 mW

# GF40: SSTL\_15 Pad Set



## Characterization Corners

Nominal VDD	Model	VDD	DVDD = 1.5V	Temperature
1.2	FF	+5%	+5%	-40°C
	FF	+5%	+5%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-5%	-40°C
	SS	-10%	-5%	125°C
1.1	FF	+10%	+5%	-40°C
	FF	+10%	+5%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-5%	-40°C
	SS	-10%	-5%	125°C

## Physical size

Name	Width	Height	Units
SLP_BI_SDS_15V_D/DVDD/DVSS/PDO	55	170	µm
SLP_CL_SDS_15V_D_PWR	110	170	µm
SLP_SP_CAL_SDS_15V	55	170	µm
SLP_RE_000_15V	27.5	170	µm
PVP_VD_RCD_1215V	27.5	170	µm
PVP_VS_RCD_1215V	27.5	170	µm
SVP_SP_000_15V	0.1	170	µm
SVP_SP_001_15V	1	170	µm
SVP_SP_005_15V	5	170	µm
SVP_SP_010_15V	10	170	µm
SPP_RS_005_15V	5	170	µm
SPP_AD_SSTL_15V	25	180	µm
SVP_CO_001_15V	170	170	µm

## Cell summary

Name	Description
SLP_BI_SDS_15V_D /DVDD/DVSS/PDO	SSTL_15 I/O pad with power
SLP_CL_SDS_15V_D_PWR	Differential clock buffer with DVDD/DVSS
SLP_SP_CAL_SDS_15V	Calibration pad
SLP_RE_000_15V	V <sub>REF</sub> pad
PVP_VD_RCD_1215V	Core V <sub>DD</sub> with VREF bus
PVP_VS_RCD_1215V	Core V <sub>SS</sub> pad with VREF bus
SVP_SP_000_15V	0.1 µm spacer
SVP_SP_001_15V	1 µm spacer
SVP_SP_005_15V	5 µm spacer
SVP_SP_010_15V	10 µm spacer
SPP_RS_005_15V	DVDD, DVSS, POC, CP[1..3], CN[1..3] and VREF rail splitter
SPP_AD_SSTL_15V	Adapter to staggered libraries
SVP_CO_001_15V	Corner cell

© 2008-2011 Aragio Solutions. All rights reserved.

Information in this document is subject to change without notice. Aragio Solutions may have patents, patent applications, trademarks, copyrights or other intellectual property rights covering subject matter in this document. Except as expressly provided in any written license agreement from Aragio, the furnishing of this document does not give you any license to the patents, trademarks, copyrights, or other intellectual property.

Published by:

**Aragio Solutions**  
2201 K Avenue  
Section B Suite 200  
Plano, TX 75074-5918  
Phone: (972) 516-0999  
Fax: (972) 516-0998  
Web: <http://www.aragio.com/>

While every precaution has been taken in the preparation of this book, the publisher assumes no responsibility for errors or omissions, or for damages resulting from the use of the information contained herein. This document may be reproduced and distributed in whole, in any medium, physical or electronic, under the terms of a license or nondisclosure agreement with Aragio.

Printed in the United States of America