GF40: Oscillators

Libraries

Name	Process	Form Factor	Silicon proven
RGO_GF40_25V33_LP_20C_OSC	LP	staggered	yes
RGO_GF40_25V33_LP_40C_OSC	LP	Inline	yes

Summary

Included are three oscillator macro I/O cells:

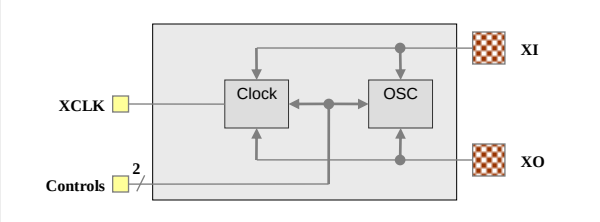
- 50 MHz oscillator
- 100 MHz oscillator
- 32 kHz oscillator

ESD Protection

I/O pads are designed with robust ESD protection for all market segments. Passed:

- 2KV ESD Human Body Model (HBM)
- 200 V ESD Machine Model (MM)
- 500 V ESD Charge Device Model (CDM)

OSx_BI_032_12V



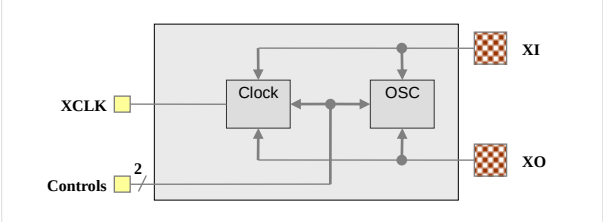
Description

The OSx_BI_032_12V oscillator is designed to generate an asynchronous on-chip clock signal with an appropriate external oscillator crystal. The design has been optimized for low power (1.5 µW typical), stability and minimum jitter using a general purpose 32KHz crystal. The design has been characterized to allow a variation of 4pF to 18pF on each pin.

Key features:

- Very low power (2.6 µW max)
- Bypass mode
- Power down (disable) mode
- Speed-up circuitry for fast startup

OSx_BI_050_12V



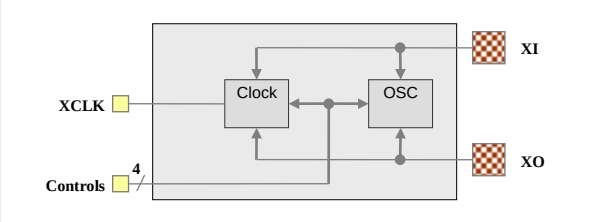
Description

The OSx_BI_050_12V oscillator is designed to generate an asynchronous on-chip clock signal with an appropriate external oscillator crystal. The design has been optimized for a wide operating range, stability and minimum jitter using a wide range of industry standard crystals. The design has been characterized to allow a variation of 4pF to 18pF on each pin.

Key features:

- Low power
- Bypass mode
- Power down (disable) mode
- Frequency range of 1 MHz to 50 MHz

OSx_BI_100_33V



Description

The OSx_BI_100_33V oscillator is designed to generate an asynchronous on-chip clock signal with an appropriate external oscillator crystal. The design has been optimized for a wide operating range, stability and minimum jitter using a wide range of industry standard crystals. The design has been characterized to allow a variation of 4pF to 18pF on each pin.

Key features:

- Programmable current for wide frequency range
- Frequency range of 1 MHz to 100 MHz
- DVDD options from 1.5V to 3.3V
- Bypass mode
- Power down (disable) mode

Recommended operating conditions

	Description	Min	Nom	Max	Units
V_{DVDD}	I/O supply voltage	2.97	3.3	3.63	V
		2.70	3.0	3.30	V
		2.52	2.8	3.08	V
		2.25	2.5	2.50	V
		1.62	1.8	1.98	V
		1.35	1.5	1.65	
T_A	Ambient operating temperature	0	25	100	°C
V_{VDD}	Core supply voltage	0.9	1.0 to 1.2	1.26	V
T_J	Junction temperature	-40	25	**+175**	°C
V_{PAD}	Voltage at PAD	0	-	V_{DVDD}	V
V_{IH}	Input logic high	0.7 * V_{DVDD}		V_{DVDD} + 0.3	V
V_{IL}	Input logic low	V_{DVSS} - 0.3		0.3 * V_{DVDD}	V

Characterization Corners

Nominal VDD	Model	VDD	DVDD[1]	Temperature
1.2	FF	+5%	+10%	-40°C
	FF	+5%	+10%	125°C/150°C/175°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C/150°C/175°C
1.0/1.1	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C/150°C/175°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C/150°C/175°C

[1] DVDD = 1.5, 1.8, 2.5, 2.8, 3.0 and 3.3V

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