

GF40: PCI 3.0



Libraries

Name	Process	Form Factor	Silicon proven
RGO_GF40_25V33V_LP_20C_PCI	LP	staggered	yes
RGO_GF40_25V33V_LP_40C_PCI	LP	Inline	yes

Summary

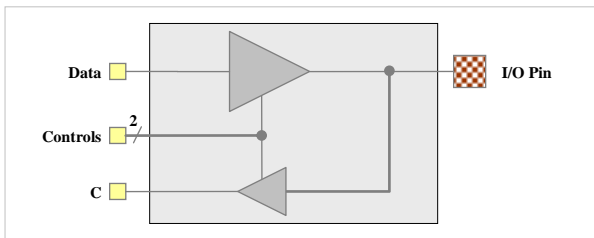
These pads are compatible with PCI Local Bus Specification Revision 3.0 for 3.3V signaling. Cell can be used for both 33MHz and 66MHz operation.

ESD Protection

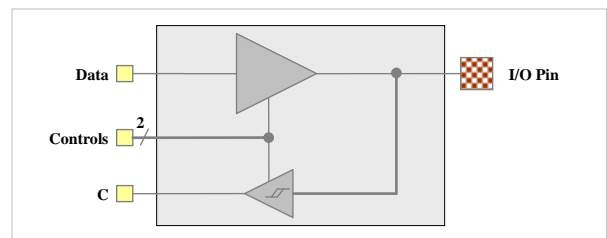
I/O pads are designed with robust ESD protection for all market segments. Passed:

- 2KV ESD Human Body Model (HBM)
- 200 V ESD Machine Model (MM)
- 500 V ESD Charge Device Model (CDM)

PCx_BI_066_33V_NCW



PCx_BI_066_33V_SCW



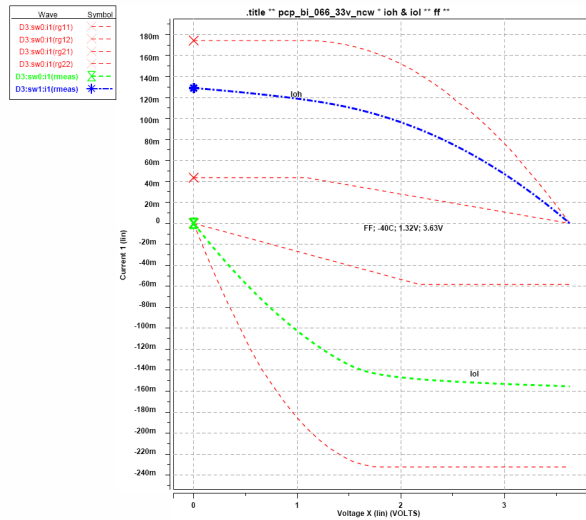
Description

PCI 3.0 pad without Schmitt trigger.

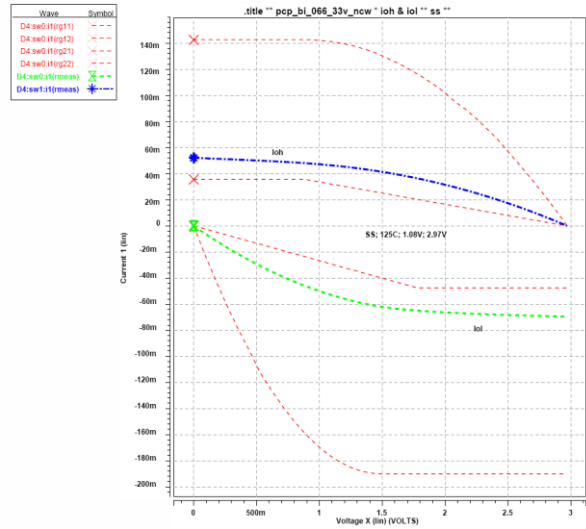
Description

PCI 3.0 pad with Schmitt trigger.

IOH / IOL (FF corner)



IOH / IOL (SS corner)



Recommended operating conditions

Description	Min	Nom	Max	Units
V _{DVDD} I/O supply voltage	2.97	3.3	3.63	V
T _A Ambient operating temperature	0	25	100	°C
V _{VDD} Core supply voltage	0.9	1.1-1.2	1.26	V
T _J Junction temperature	-40	25	125	°C
V _{PAD} Voltage at PAD	0	-	V _{DVDD}	V
V _{IH} Input logic high	0.7 * V _{DVDD}		V _{DVDD} + 0.3	V
V _{IL} Input logic low	V _{DVSS} - 0.3		0.3 * V _{DVDD}	V

Characterization Corners

Nominal VDD	Model	VDD	DVDD=3.3V	Temperature
1.1-1.2	FF	+5%	+10%	-40°C
	FF	+5%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C

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