GF40: 3.3V GPIO

Libraries

Name	Process	Form Factor	Silicon proven
RGO_GF40_25V33_LP_20C	LP	staggered	yes
RGO_GF40_25V33_LP_40C	LP	Inline	yes

Summary

A full range of power pads is provided to enable the system designer different options for separate core power (VDD and VSS) and separate I/O padring power and ground (DVDD and DVSS). The ability to isolate separate power domains is also provided. In addition, the I/O library has a full complement of cells that provide the user with the ability to isolate analog I/O's and power within the same padring as the digital I/O's.
Includes:

- Programmable GPIO
- Programmable fault-tolerant GPIO
- Input buffer
- Power supplies
- Isolated analog power supplies
- Oscillators
- Full complement of support pads

ESD Protection

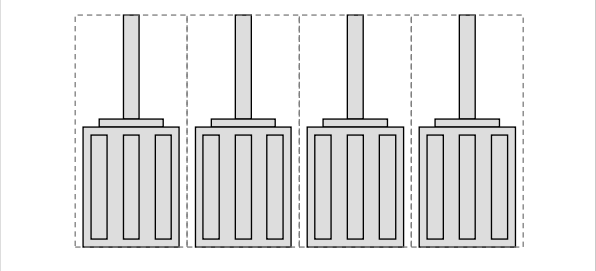
I/O pads are designed with robust ESD protection for all market segments. Passed:

- 2KV ESD Human Body Model (HBM)
- 200 V ESD Machine Model (MM)
- 500 V ESD Charge Device Model (CDM)

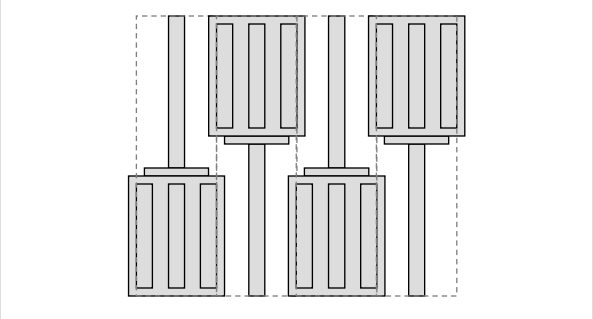
Form factor

Libraries are offered in both inline (core-limited) and staggered (pad limited) configurations.

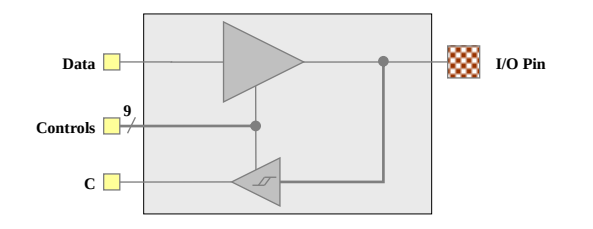
Inline (core-limited) – 44µm x 92µm



Staggered (pad-limited) – 20µm x 180µm



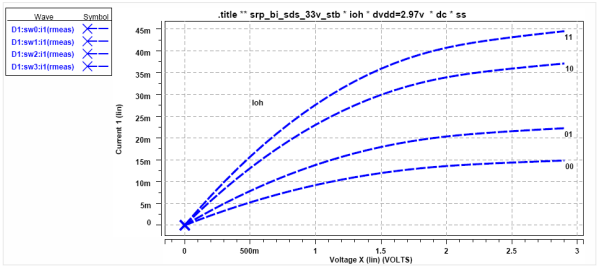
SRx_BI_SDS_33V_STB / FRx_BI_SDS_33V_STB



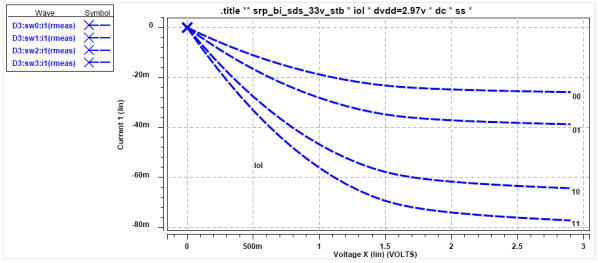
Description

SRx_BI_SDS_33V_STB / FRx_BI_SDS_33V_STB are programmable, multi-voltage (1.8V, 2.5V, 2.8V, 3.0V, 3.3V) general purpose, bi-directional I/O buffers with a selectable LVCMOS input or LVCMOS Schmitt trigger input and programmable pull-up / pull-down. In the full-drive mode, this buffer can operate in excess of 100MHz frequency with 15pF external load and 125 MHz with 10pF load, but actual frequency is load and system dependent. A maximum of 200 MHz can be achieved under small capacitive loads.

I_{OH} (DVDD = 2.97V, SS)



I_{OL} (DVDD = 2.97V, SS)



Recommended operating conditions

	Description	Min	Nom	Max	Units
V_{DVDD}	I/O supply voltage	2.97	3.3	3.63	V
		2.70	3.0	3.30	V
		2.52	2.8	3.08	V
		2.25	2.5	2.50	V
		1.62	1.8	1.98	V
T_A	Ambient operating temperature	0	25	100	°C
V_{VDD}	Core supply voltage	0.9	1.0 to 1.2	1.26	V
T_J	Junction temperature	-40	+25	**+175**	°C
V_{PAD}	Voltage at PAD	0	-	V_{DVDD}	V
V_{IH}	Input logic high	0.7 * V_{DVDD}		V_{DVDD} + 0.3	V
V_{IL}	Input logic low	V_{DVSS} - 0.3		0.3 * V_{DVDD}	V

Characterization Corners

Nominal VDD	Model	VDD	DVDD[1]	Temperature
1.2	FF	+5%	+10%	-40°C
	FFF	+5%	+10%	125°C
	FFF	+5%	+10%	150°C
	FFF	+5%	+10%	175°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
	SS	-10%	-10%	150°C
	SS	-10%	-10%	175°C
1.1/1.0	FF	+10%	+10%	-40°C
	FFF	+10%	+10%	125°C
	FFF	+10%	+10%	150°C
	FFF	+10%	+10%	175°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
	SS	-10%	-10%	150°C
	SS	-10%	-10%	175°C

[1] DVDD = 1.8, 2.5, 2.8, 3.0 and 3.3V

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