

Libraries

Name	Process	Form Factor
RGO_SMIC40_25V25_LL_UC_LVDS	LL	Staggered CUP

Summary

The LVDS library provides an LVDS driver, receiver, and temperature stable voltage reference capable of supporting 16 drivers operating at data rates up to 2.0 Gbps. The pad set includes a full complement of power, spacer, and adapter cells to assemble a complete pad ring by abutment. An included rail splitter allows isolated LVDS domains to be placed in the same pad ring with other power domains while maintaining continuous VDD/VSS in the pad ring for robust ESD protection.

- 1.0 GHz LVDS Driver
- 1.0 GHz LVDS Receiver
- LVDS Voltage Reference

LVDS Specification Compliant:

- TIA/EIA-644-A - Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits
- IEEE Std 1596.3-1996

ESD Protection:

- JEDEC compliant
 - 2KV ESD Human Body Model (HBM)
 - 200 V ESD Machine Model (MM)
 - 500 V ESD Charge Device Model (CDM)

Latch-up Immunity:

- JEDEC compliant
 - Tested to I-Test criteria of $\pm 100\text{mA}$ @ 125°C

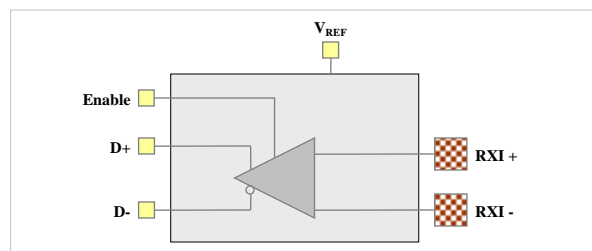
Recommended operating conditions

Symbol	Description	Min	Nom	Max	Units
V_{VDD}	Core supply voltage	0.99	1.1	1.21	V
V_{DVDD}	I/O supply voltage	2.25	2.5	2.75	V
T_{J}	Junction temperature	-40	25	125	$^\circ\text{C}$
V_{PAD}	Voltage at PAD	-0.3V		$V_{\text{DVDD}}+0.3\text{V}$	V

Characterization Corners

Nominal VDD	Model	VDD	DVDD = 2.5V	Temperature
1.1	FF	+10%	+10%	-40 $^\circ\text{C}$
	FF	+10%	+10%	125 $^\circ\text{C}$
	TT	nominal	nominal	25 $^\circ\text{C}$
	SS	-10%	-10%	-40 $^\circ\text{C}$
	SS	-10%	-10%	125 $^\circ\text{C}$

LDP_IN_675_25V_DN: 1GHz LVDS Input



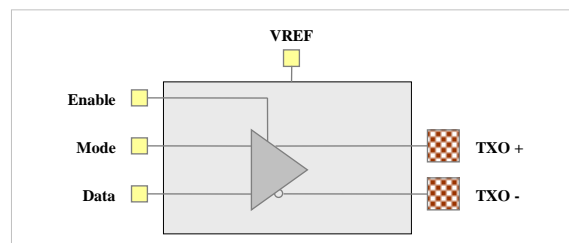
LVDS Receiver Features:

- Input receive sensitivity of 75mV peak differential (without hysteresis)
- Common mode range from 0V to 2.4V (limited by Power Supply)
- Powered by 2.5V I/O and 1.1V core supplies
- Power consumption: 5 mW typ & 8.5 mW max @ 1GHz

AC Characteristics

Parameter	Typ	Max	Units	Conditions
Propagation delay	0.5	0.85	ns	The slew rate for propagation delays, duty cycle distortion and maximum operating frequency are 1V/ns
Maximum operating frequency	1		GHz	All noise, jitter, and t _{dc} measured at 1GHz
Maximum data rate	2		Gb/s	

LDP_OU_675_25V_T: 1GHz LVDS Output



LVDS Driver Features:

- Operates up to 1GHz (2Gbps) with external 1 pF load
- Common mode output range 1.2V \pm 100mV
- Differential Skew between TXO_P and TXO_N 20ps
- High and low current drive modes to support 50 Ω and 100 Ω differential terminations
- Powered by 2.5V I/O and 1.1V core supplies
- Power consumption: 18.1 mW typ & 25.2 mW max

AC Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
t_{PHL}	Differential high to low propagation delay	$R_{\text{L}} = 100 \Omega$ $C_{\text{L}} = 1 \text{ pF}$	450	690		ps
t_{PLH}	Differential low to high propagation delay	$R_{\text{L}} = 100 \Omega$ $C_{\text{L}} = 1 \text{ pF}$	450	687		ps
t_{rise}	V_{OD} differential rise time	20% to 80%	150	170	200	ps
t_{fall}	V_{OD} differential fall time	20% to 80%	150	170	200	ps

Cell summary

Name	Description
LDP_IN_675_25V_DN	1GHz LVDS input cell
LDP_OU_675_25V_T	1GHz LVDS output cell
LDP_RE_000_25V	LVDS Voltage Reference cell
PVP_VD_RCD_12V	Core power (VDD)
PVP_VS_RCD_12V	Core ground (VSS)
PVP_VD_PDO_25V	I/O power (DVDD) with POC control
PVP_VD_RDO_25V	I/O power (DVDD)
PVP_VS_RDO_25V	I/O ground (VSS)
SVP_SP_000_25V	0.1 μ m spacer
SVP_SP_001_25V	1 μ m spacer
SVP_SP_005_25V	5 μ m spacer
SVP_SP_010_25V	10 μ m spacer
SPP_RS_005_25V	DVDD, DVSS, POC, BIAS and VREF rail splitter
SPC_SPP_AD_UN	Inline to staggered adapter

Physical sizes

Pad name	Width	Height[*]	Units
LDP_RE_000_18V	37	180	μ m
LDP_IN_675_25V_DN	55	180	μ m
LDP_OU_675_25V_T	55	180	μ m
PVP_VD_RCD_12V	20	180	μ m
PVP_VS_RCD_12V	20	180	μ m
PVP_VD_PDO_25V	20	180	μ m
PVP_VD_RDO_25V	20	180	μ m
PVP_VS_RDO_25V	20	180	μ m
SVP_SP_000_25V	0.1	180	μ m
SVP_SP_001_25V	1	180	μ m
SVP_SP_005_25V	5	180	μ m
SVP_SP_010_25V	10	180	μ m
SPP_RS_005_25V	5	180	μ m
SPC_SPP_AD_UN	25	180	μ m

[*] Includes CUP bond opening.

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