

Libraries

Name	Process	Form Factor
RGO_TSMC16_18V15_FFC_25C_DDR4_7WC	FFC	Staggered CUP

Summary

The LPDDR2/3_DDR3/4 libraries contain the 6-way combo driver/receiver cells with embedded power cells, the driver impedance calibration cell, and the DDR voltage reference cell providing both single-ended and differential signaling for LPDDR2, LPDDR3, LPDDR4, DDR3, DDR3L, DDR3U, and DDR4 applications. Also included is a full complement of power, corner and spacer cells to assemble a complete pad ring by abutment. An included rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

Full DDR4 capability

- Data rates – 1600 MT/s, 1866 MT/s, 2133 MT/s, 2400 MT/s

Full DDR3 / DDR3L / DDR3U capability

- Data rates – 800 MT/s, 1066 MT/s, 1333 MT/s, 1600 MT/s, 1866 MT/s, 2133 MT/s

Full LPDDR4 capability

- Data rates – 1066 MT/sec, 2400 MT/sec, 3200 MT/sec, 4266 MT/sec

Full LPDDR3 capability

- Data rates – 1333 MT/sec, 1600 MT/sec

Full LPDDR2 capability

- Data rates – 466 MT/sec, 1066 MT/sec

ESD Protection:

- JEDEC compliant
 - 2KV ESD Human Body Model (HBM)
 - 200 V ESD Machine Model (MM)
 - 500 V ESD Charge Device Model (CDM)

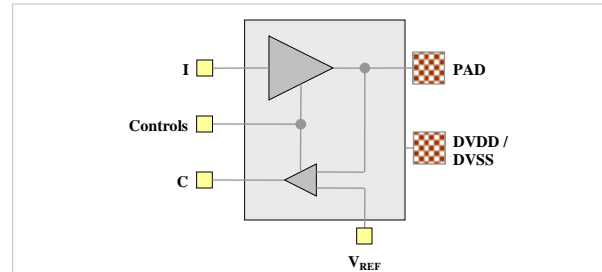
Latch-up Immunity:

- JEDEC compliant
 - Tested to I-Test criteria of $\pm 100\text{mA}$ @ 125°C

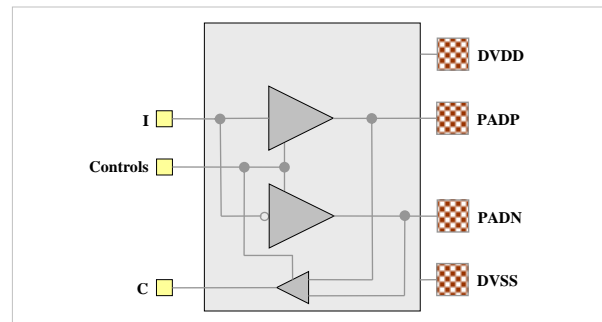
Recommended operating conditions

Parameter	Description	Min	Nom	Max	Units			
V _{VDD}	Core supply voltage	0.72	0.80	0.88	V			
		DDR4	1.14	1.2	1.26	V		
		DDR3	1.425	1.5	1.575	V		
		DDR3L	1.283	1.35	1.45	V		
		V _{DVDD}	I/O supply voltage	DDR3U	1.19	1.25	1.31	V
				LPDDR2	1.14	1.2	1.3	V
LPDDR3	1.14			1.2	1.3	V		
	LPDDR4	1.06	1.1	1.17	V			
T _J	Junction temperature	-40	25	+125	°C			
V _{PAD}	Voltage at PAD	V _{DVSS}		V _{DVDD}	V			

SLP_BI_SDS_1215V_D_x: Single-Ended Driver



SLP_CL_SDS_1215V_D_PWR : Differential Driver



Product Features

- User programmable drive strength
 - DDR3 – Z_{OUT} = 34 / 40 Ω
 - DDR4 – Z_{OUT} = 34 / 48 Ω
 - LPDDR2 – Z_{OUT} = 34 / 40 / 48 / 60 / 80 Ω
 - LPDDR3 – Z_{OUT} = 34 / 40 Ω
 - LPDDR4 – Z_{OUT} = 40 / 48 / 60 / 80 / 120 / 240 Ω
- User programmable on-die termination
 - DDR3 – 120 / 60 / 40 / 30 / 24 / 20 / 17 Ω
 - DDR4 – 240 / 120 / 80 / 60 / 48 / 40 / 34 Ω
 - LPDDR3 – 240 / 120 / 80 / 60 / 48 / 40 / 34 Ω
 - LPDDR4 – 240 / 120 / 80 / 60 / 48 / 40 / 34 Ω
- Operating frequency up to 2133 MHz (4266 MT/sec) data rate)

Characterization Corners

Model	LPE Type	VDD=0.8V	DVDD [1]	Temp
FFGNP	Cbest_CCbest_T	+10%	+10%	-40°C
FFGNP	Cbest_CCbest_T	+10%	+10%	0°C
FFGNP	Cbest_CCbest_T	+10%	+10%	125°C
FFG	Ctypical	+10%	+10%	125°C
TT	Ctypical	nominal	nominal	25°C
TT	Ctypical	nominal	nominal	85°C
SSGNP	Cworst_CCworst_T	-10%	-10%	-40°C
SSGNP	Cworst_CCworst_T	-10%	-10%	0°C
SSGNP	Cworst_CCworst_T	-10%	-10%	125°C

[1] DVDD = 1.1V, 1.2V, 1.25V, 1.35V, 1.5V

Cell summary

Name	Description
SLP_BI_SDS_1215V_D_DVDD/DVSS/PDO *	Bi-directional driver / receiver cell with power
SLP_CL_SDS_1215V_D_PWR *	Differential clock driver / receiver with DVDD / DVSS
SLP_SP_CAL_SDS_1215V *	DDR3 / DDR4 calibration pad
SLP_SP_CSH_0915V *	Calibration code bus driver
SLP_RE_000_1215V *	DDR3 / DDR4 voltage reference
PVP_VD_RCD_0915V	Core power (VDD)
PVP_VS_RCD_0915V	Core ground (VSS)
SVP_SP_000_1215V	0.1 μ m spacer
SVP_SP_001_1215V	1 μ m spacer
SVP_SP_005_1215V	5 μ m spacer
SVP_SP_020_1215V	20 μ m spacer
SVP_CO_001_1215V	Corner cell
SPP_RS_005_1215V	Rail splitter
SPP_AD_SSTL_1215V	DDR to staggered 1.8V GPIO adapter
SPP_SP_CAP_1215V	DVDD/DVSS decoupling cap

* Vertical-only and horizontal-only orientations

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