

TSMC16: 1.8V GPIO



Libraries

Name	Process	Form Factor
RG0_TSMC16_18V18_FFC_20C	FFC	Staggered CUP

Summary

The 1.8V General Purpose I/O library provides bidirectional I/O, isolated analog I/O, and a full complement of power cells along with corner and spacer cells to assemble a complete pad ring by abutment. An included rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

- Programmable bidirectional GPIO
- Input-only buffer
- Isolated analog I/O
- Full complement of power, corner, and spacer cells

ESD Protection:

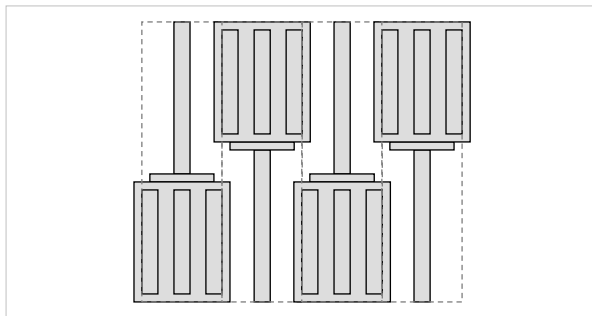
- JEDEC compliant
 - 2KV ESD Human Body Model (HBM)
 - 200 V ESD Machine Model (MM)
 - 500 V ESD Charge Device Model (CDM)

Latch-up Immunity:

- JEDEC compliant
 - Tested to I-Test criteria of $\pm 100\text{mA}$ @ 125°C

Cell Size & Form Factor

Staggered (pad-limited) – $25\mu\text{m} \times 165\mu\text{m}$

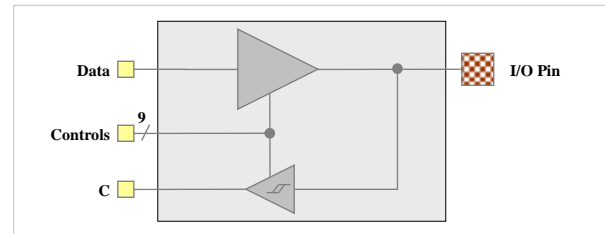


- Vertical-only and horizontal-only orientations

Recommended operating conditions

Description	Min	Nom	Max	Units
V_{VDD} Core supply voltage	0.72	0.80	0.88	V
V_{DVDD} I/O supply voltage	1.35	1.5	1.65	V
T_{J} Junction temperature	-40	25	125	$^\circ\text{C}$
V_{PAD} Voltage at PAD	$V_{\text{DVSS}} - 0.3$	-	$V_{\text{DVDD}} + 0.3$	V

SRP_BI_SDS_18V_STB

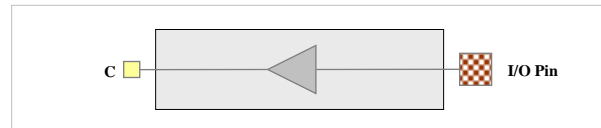


Bidirectional GPIO Driver Features

- Multi-Voltage (1.5V, 1.8V)
- LVCMOS / LVTTTL input with selectable hysteresis
- Programmable drive strength (rated 2mA to 12mA)
- Selectable output slew rate
- Optimized for EMC with SSO factor of 8
- Open-drain output mode
- Programmable input options (pull-up/pull-down/repeater)
- Power-On Start (POS) capable
- Power sequencing independent design with Power-On Control

In full-drive mode, this driver can operate to frequencies in excess of 100MHz with 15pF external load and 125 MHz with 10pF load. Actual frequency limits are load and system dependent. A maximum of 200 MHz can be achieved under small capacitive loads.

STP_IN_001_18V_NC



Input-Only GPIO Features

- Multi-voltage (1.5V, 1.8V)
- Wide input slew-rate
- LVCMOS/LVTTL compatible input with no hysteresis
- Minimized skew for optimum performance over frequency
- No power sequence requirements

Characterization Corners

Model	LPE Type	VDD=0.8V	DVDD [1]	Temp
FFGNP	Cbest_CCbest_T	+10%	+10%	-40 $^\circ\text{C}$
FFGNP	Cbest_CCbest_T	+10%	+10%	0 $^\circ\text{C}$
FFGNP	Cbest_CCbest_T	+10%	+10%	125 $^\circ\text{C}$
FFG	Ctypical	+10%	+10%	125 $^\circ\text{C}$
TT	Ctypical	nominal	nominal	25 $^\circ\text{C}$
TT	Ctypical	nominal	nominal	85 $^\circ\text{C}$
SSGNP	Cworst_CCworst_T	-10%	-10%	-40 $^\circ\text{C}$
SSGNP	Cworst_CCworst_T	-10%	-10%	0 $^\circ\text{C}$
SSGNP	Cworst_CCworst_T	-10%	-10%	125 $^\circ\text{C}$

[1] DVDD = 1.5V & 1.8V

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