

Libraries

Name	Process	Form Factor
RGO_TSMC28_18V18_HPM_20C_ONFI_3	HPM	Staggered CUP

Summary

The ONFI 3.0 library provides the combo driver / receiver cells, the ODT / driver impedance calibration cell, and the voltage reference cell to support both single-ended and differential ONFI 3.0 signaling. This library also meets the requirements for Toggle 2.0 signaling. The pad set includes a full complement of power, spacer, and adapter cells to assemble a complete pad ring by abutment. An included rail splitter allows isolated ONFI domains to be placed in the same pad ring with other power domains while maintaining continuous VDD/VSS in the pad ring for robust ESD protection.

- ONFI 3.0 Single-Ended Driver /Receiver
- ONFI 3.0 Differential Clock Driver / Receiver
- ODT / Z_o Calibration Cell
- Voltage Reference

The ONFI 3.0 I/O library supports all impedance modes defined in the ONFI 3.0 specification and features fast and precise calibration, low power consumption, area-efficient design, and easy integration into the physical layer (PHY).

ESD Protection:

- JEDEC compliant
 - 2KV ESD Human Body Model (HBM)
 - 200 V ESD Machine Model (MM)
 - 500 V ESD Charge Device Model (CDM)

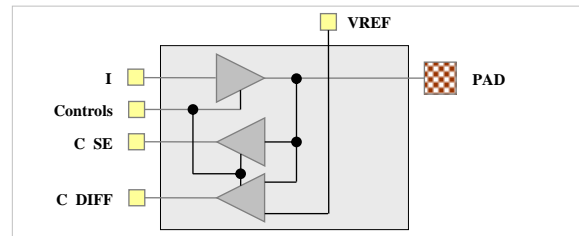
Latch-up Immunity:

- JEDEC compliant
 - Tested to I-Test criteria of $\pm 100\text{mA}$ @ 125°C

Recommended operating conditions

Symbol	Description	Min	Nom	Max	Units
V_{DD}	Core supply voltage	0.81	0.9	0.99	V
T_J	Junction temperature	-40	25	125	$^\circ\text{C}$
V_{PAD}	Voltage at PAD	-0.3V		$V_{DVDD}+0.3V$	V
V_{DVDD}	I/O supply voltage	1.62	1.8	1.98	V
$V_{IH(DC)}$	Input High (DC)	NV-DDR	$0.7 * V_{DVDD}$	$V_{DVDD} + 0.3$	V
$V_{IL(DC)}$	Input Low (DC)		$V_{DVSS} - 0.3$	$0.3 * V_{DVDD}$	V
$V_{IH(AC)}$	Input High (AC)	NV-DDR	$0.8 * V_{DVDD}$	$V_{DVDD} + 0.3$	V
$V_{IL(AC)}$	Input Low (AC)		$V_{DVSS} - 0.3$	$0.2 * V_{DVDD}$	V
V_{DVDD}	I/O supply voltage	1.62	1.8	1.98	V
$V_{IH(DC)}$	Input High (DC)	NV-DDR2	$V_{REF} + .125$	$V_{DVDD} + 0.3$	V
$V_{IL(DC)}$	Input Low (DC)		$V_{DVSS} - 0.3$	$V_{REF} -.125$	V
$V_{IH(AC)}$	Input High (AC)	NV-DDR2	$V_{REF} +.250$		V
$V_{IL(AC)}$	Input Low (AC)			$V_{REF} -.125$	V

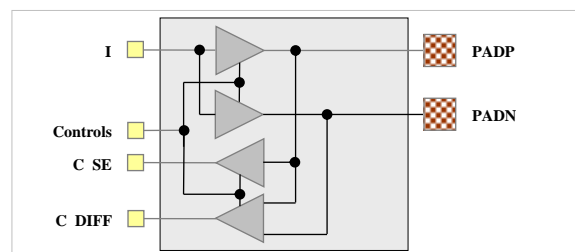
ONP_BI_SDS_18V_SCB: Single-Ended Driver



ONFI Single-Ended Driver / Receiver Features:

- Driver – user-selectable on-die termination and programmable drive strength with ODT / Z_o calibration and programmable “off” state control.
 - ODT $R_{it} = 30\Omega / 50\Omega / 75\Omega / 100\Omega / 150\Omega$
 - $Z_{OUT} = 18\Omega / 25\Omega / 35\Omega / 50\Omega$
 - Off state – $Z /$ pull-up / pull-down / bus keeper
- Receiver – single-ended and pseudo-differential outputs
- Powered by 1.8V I/O and 0.9V core supplies
- Maximum operating frequency – 266 MHz

ONP_CL_SDS_18V_SCB: Differential Driver



ONFI Differential Clock Driver / Receiver Features:

- Driver – user-selectable on-die termination and programmable drive strength with ODT / Z_o calibration and programmable “off” state control.
 - ODT $R_{it} = 30\Omega / 50\Omega / 75\Omega / 100\Omega / 150\Omega$
 - $Z_{OUT} = 18\Omega / 25\Omega / 35\Omega / 50\Omega$
 - Off state – $Z /$ pull-up / pull-down / bus keeper
- Receiver – single-ended and true differential outputs
- Powered by 1.8V I/O and 0.9V core supplies
- Maximum operating frequency – 266 MHz

Characterization Corners

Nominal VDD	Model	VDD	DVDD=1.8V	Temperature
0.9V	FF	+10%	+10%	-40 $^\circ\text{C}$
	FF	+10%	+10%	0 $^\circ\text{C}$
	FF	+10%	+10%	125 $^\circ\text{C}$
	TT	nominal	nominal	25 $^\circ\text{C}$
	SS	-10%	-10%	-40 $^\circ\text{C}$
	SS	-10%	-10%	125 $^\circ\text{C}$

Partial set represented – see datasheet for complete detail.

Cell summary

Name	Description
ONP_BI_SDS_18V_SCB *	ONFI Single-Ended Driver/Receiver
ONP_CL_SDS_18V_SCB *	ONFI Differential Clock Driver/Receiver
ONP_SP_CAL_18V *	Calibration cell
ONP_RE_000_18V *	Voltage Reference (VREF).
FVP_VD_PDO_1018V *	I/O V _{DD} (DVDD) with POC
FVP_VD_RDO_1018V	I/O V _{DD} (DVDD)
FVP_VS_RDO_1018V	I/O V _{SS} (DVSS)
FVP_VS_DRC_18V	I/O V _{SS} (DVSS is shorted to VSS)
FVP_VD_RCD_1018V	Core V _{DD} (VDD)
FVP_VS_RCD_1018V	Core V _{SS} (VSS)
FVP_VS_DRC_1018V	Core V _{SS} (DVSS is shorted to VSS)
SVP_CO_001_1018V	Corner cell
SVP_SP_001_1018V	1 μ m spacer cell
SVP_SP_005_1018V	5 μ m spacer cell
SVP_SP_020_1018V	20 μ m spacer cell
SPP_RS_005_1018V	Rail splitter cell (breaks DVDD, DVSS, VREF, CAL_DWHVx[3:0], POC and HVPS)
SPP_SP_CAP_1018V	Core decap cell

* Vertical-only and horizontal-only orientations

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