

Libraries

Name	Process	Form Factor
RGO_TSMC28_18V25_HPM_UC_LVDS	HPM	Staggered CUP

Summary

The LVDS library provides an LVDS driver, receiver, and temperature stable voltage reference capable of supporting 16 drivers operating at data rates up to 2.4 Gbps. The pad set includes a full complement of power, spacer, and adapter cells to assemble a complete pad ring by abutment. An included rail splitter allows isolated LVDS domains to be placed in the same pad ring with other power domains while maintaining continuous VDD/VSS in the pad ring for robust ESD protection.

- 1.0 GHz LVDS Driver
- 1.2 GHz LVDS Receiver
- LVDS Voltage Reference

LVDS Specification Compliant:

- TIA/EIA-644-A - Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits
- IEEE Std 1596.3-1996

ESD Protection:

- JEDEC compliant
 - 2KV ESD Human Body Model (HBM)
 - 200 V ESD Machine Model (MM)
 - 500 V ESD Charge Device Model (CDM)

Latch-up Immunity:

- JEDEC compliant
 - Tested to I-Test criteria of $\pm 100\text{mA}$ @ 125°C

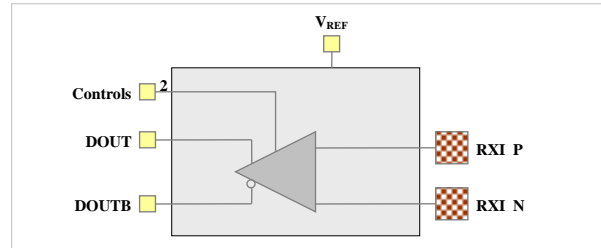
Recommended operating conditions

Symbol	Description	Min	Nom	Max	Units
V_{VDD}	Core supply voltage	0.81	0.9	0.99	V
V_{DVDD}	I/O supply voltage	1.62	1.8	1.98	V
T_{J}	Junction temperature	-40	25	125	$^\circ\text{C}$
V_{PAD}	Voltage at PAD	-0.3V		$V_{\text{DVDD}}+0.3\text{V}$	V

Characterization Corners

Nominal VDD	Model	VDD	DVDD = 1.8V	Temperature
0.9V	FF	+10%	+10%	-40 $^\circ\text{C}$
	FF	+10%	+10%	125 $^\circ\text{C}$
	TT	nominal	nominal	25 $^\circ\text{C}$
	SS	-10%	-10%	-40 $^\circ\text{C}$
	SS	-10%	-10%	125 $^\circ\text{C}$

LDP_IN_800_25V_DN: 1.2GHz LVDS Receiver



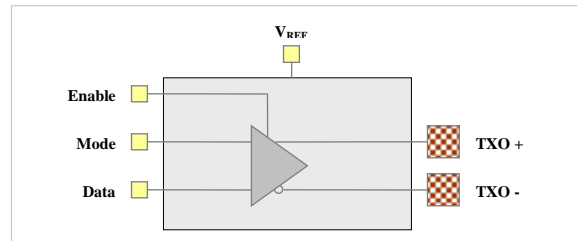
LVDS Receiver Features:

- Input receive sensitivity of 75mV peak differential (without hysteresis)
- Common mode range from 0V to 1.8V (limited by power supply)
- Powered by 1.8V I/O and 0.9V core supplies
- Power consumption: 7.7 mW max @ 1.2GHz

AC Characteristics

Parameter	Typ	Max	Units	Conditions
Propagation delay	0.5	0.65	ns	The slew rate for propagation delays, duty cycle distortion and maximum operating frequency are 1V/ns
Maximum operating frequency	1.2		GHz	All noise, jitter, and tdc measured at 1GHz
Maximum data rate	2.4		Gb/s	

LDP_OU_800_18V_T: 1.0GHz LVDS Driver



LVDS Driver Features:

- Operates up to 1.0GHz (2.0Gbps) with external 1 pF load
- Common mode output range 1.1V $\pm 100\text{mV}$
- Differential Skew between TXO_P and TXO_N 7ps
- High and low current drive modes to support 50 Ω and 100 Ω differential terminations
- Powered by 1.8V I/O and 0.9V core supplies
- Power consumption: 17.1 mW max

AC Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
t_{PHL}	Differential high to low propagation delay	$R_{\text{L}} = 100 \Omega$ $C_{\text{L}} = 1 \text{ pF}$	3.0	349		ps
t_{PLH}	Differential low to high propagation delay	$R_{\text{L}} = 100 \Omega$ $C_{\text{L}} = 1 \text{ pF}$	3.0	351		ps
t_{rise}	V_{OD} differential rise time	20% to 80%	110	130		ps
t_{fall}	V_{OD} differential fall time	20% to 80%	110	130		ps

Cell Summary & Physical Sizes

Name	Description	Width (µm)	Height (µm)
LDP_IN_800_25V_DN *	1GHz LVDS input cell	50	125
LDP_OU_800_18V_T *	1GHz LVDS output cell	50	125
LDP_RE_000_18V *	LVDS Voltage Reference cell	50	125
FVP_VD_RCD_10V	Core power (VDD)	25	125
FVP_VS_RCD_10V	Core ground (VSS)	25	125
FVP_VD_PDO_18V *	I/O power (DVDD) with POC control	25	125
FVP_VD_RDO_18V	I/O power (DVDD)	25	125
FVP_VS_RDO_18V	I/O ground (VSS)	25	125
SVP_SP_000_18V	0.1 µm spacer	0.1	125
SVP_SP_001_18V	1 µm spacer	1	125
SVP_SP_005_18V	5 µm spacer	5	125
SVP_SP_010_18V	10 µm spacer	10	125
SPP_RS_005_18V	DVDD, DVSS, POC, BIAS & VREF rail splitter	5	125

*Supplied in vertical-only and horizontal-only orientations

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