TSMC28: DDR3_DDR4

Libraries

Name	Process	Form Factor
RGO_TSMC28_18V15_HPM_20C_DDR3_DDR4	HPM	Flip Chip

Summary

The DDR3_DDR4 library contains the combo driver/receiver cells with embedded power cells, the driver impedance calibration cell, and the DDR voltage reference cell providing both single-ended and differential signaling for DDR3 and DDR4 applications. Also included is a full complement of power, corner and spacer cells to assemble a complete pad ring by abutment. An included rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

Full DDR4 capability

- Data rates – 1600 MT/s, 1866 MT/s, 2133 MT/s, 2400 MT/s

Full DDR3 capability

- Data rates – 800 MT/s, 1066 MT/s, 1333 MT/s, 1600 MT/s, 1866 MT/s, 2133 MT/s

ESD Protection:

- JEDEC compliant
  - 2KV ESD Human Body Model (HBM)
  - 200 V ESD Machine Model (MM)
  - 500 V ESD Charge Device Model (CDM)

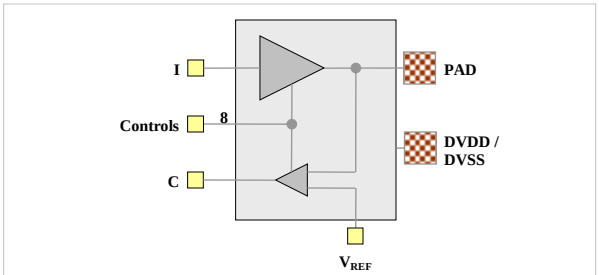
Latch-up Immunity:

- JEDEC compliant
  - Tested to I-Test criteria of ± 100mA @ 125°C

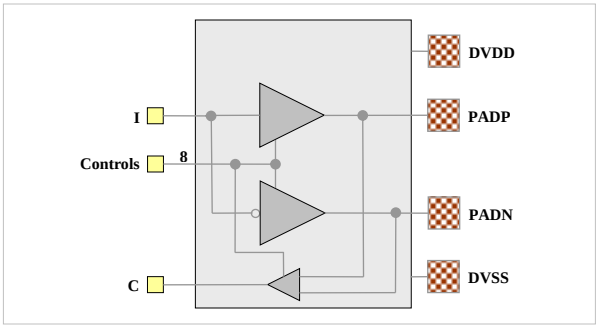
Recommended operating conditions

Parameter	Description		Min	Nom	Max	Units
V_{VDD}	Core supply voltage		0.81	0.90	0.99	V
V_{DVDD}	I/O supply voltage	DDR4	1.14	1.2	1.26	V
		DDR3	1.425	1.5	1.575	V
T_J	Junction temperature		-40	25	+125	°C
V_{PAD}	Voltage at PAD		V_{DVSS}		V_{DVDD}	V

SLP_BI_SDS_1215V_D_x: Single-Ended Driver



SLP_CL_SDS_1215V_D_PWR : Differential Driver



Product Features

- Drive strength – Z_{OUT} = 34 Ω
- User programmable on-die termination
  - DDR3 – 120 / 60 / 40 / 30 / 20 Ω
  - DDR4 – 240 / 120 / 80 / 60 / 40 Ω
- Operating frequency up to 1200 MHz (2400 MT/sec data rate)

Cell Summary & Physical Sizes

Name	Description	Width (µm)	Height (µm)
SLP_BI_SDS_1215V_D_DVDD/DVSS/PDO *	Bi-directional driver / receiver cell with power	40	205
SLP_CL_SDS_1215V_D_PWR *	Differential clock driver / receiver with DVDD / DVSS	80	205
SLP_SP_CAL_SDS_1215V *	DDR3 / DDR4 calibration pad	40	205
SLP_SP_CSH_0915V *	Calibration code bus driver	20	205
SLP_RE_000_1215V *	DDR3 / DDR4 voltage reference	40	205
PVP_VD_RCD_0915V	Core power (VDD)	20	205
PVP_VS_RCD_0915V	Core ground (VSS)	20	205
SVP_SP_000_1215V	0.1 µm spacer	0.1	205
SVP_SP_001_1215V	1 µm spacer	1	205
SVP_SP_005_1215V	5 µm spacer	5	205
SVP_SP_020_1215V	20 µm spacer	20	205
SVP_CO_001_1215V	Corner cell	205	205
SPP_RS_005_1215V	Rail splitter	5	205
SPP_AD_SSTL_1215V	DDR to staggered 1.8V GPIO adapter	20	205
SPP_SP_CAP_1215V	DVDD/DVSS decoupling cap	10	10

*Supplied in vertical-only and horizontal-only orientations

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