TSMC28: LPDDR2/3_DDR3/4

Libraries

Name	Process	Form Factor
RGO_TSMC28_18V15_HPM_25C_LPDDR3_DDR4	HPM	Staggered CUP
RGO_TSMC28_18V15_HPC_25C_LPDDR3_DDR4	HPC	Staggered CUP

Summary

The LPDDR2/3_DDR3/4 libraries contain the 6-way combo driver/receiver cells with embedded power cells, the driver impedance calibration cell, and the DDR voltage reference cell providing both single-ended and differential signaling for LPDDR2, LPDDR3, DDR3, DDR3L, DDR3U, and DDR4 applications. Also included is a full complement of power, corner and spacer cells to assemble a complete pad ring by abutment. An included rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

Full DDR4 capability
- Data rates – 1600 MT/s, 1866 MT/s, 2133 MT/s, 2400 MT/s

Full DDR3 / DDR3L / DDR3U capability
- Data rates – 800 MT/s, 1066 MT/s, 1333 MT/s, 1600 MT/s, 1866 MT/s, 2133 MT/s

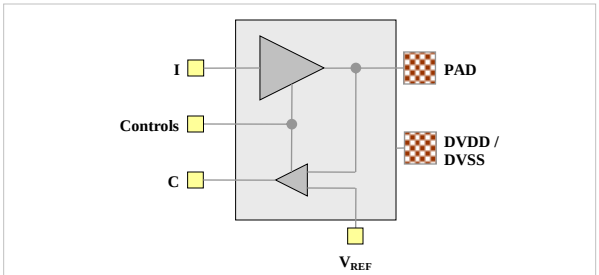
Full LPDDR3 capability
- Data rates – 1333 MT/sec, 1600 MT/sec

Full LPDDR2 capability
- Data rates – 466 MT/sec, 1066 MT/sec

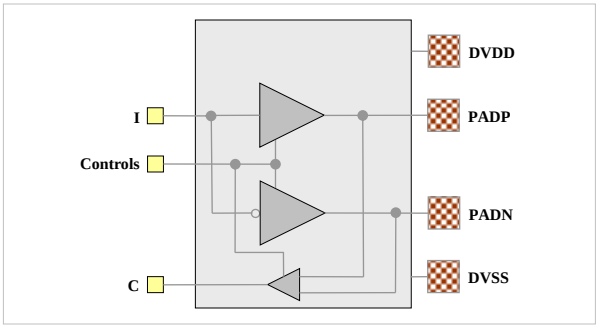
ESD Protection:
- JEDEC compliant
  - 2KV ESD Human Body Model (HBM)
  - 200 V ESD Machine Model (MM)
  - 500 V ESD Charge Device Model (CDM)

Latch-up Immunity:
- JEDEC compliant
  - Tested to I-Test criteria of ± 100mA @ 125°C

SLP_BI_SDS_1215V_D _x: Single-Ended Driver



SLP_CL_SDS_1215V_D_PWR : Differential Driver



Product Features

- User programmable drive strength
  - DDR3 – Z_{OUT} = 34 / 40 Ω
  - DDR4 – Z_{OUT} = 34 / 48 Ω
  - LPDDR2 – Z_{OUT} = 34 / 40 / 48 / 60 / 80 Ω
  - LPDDR3 – Z_{OUT} = 34 / 40 Ω
- User programmable on-die termination
  - DDR3 – 120 / 60 / 40 / 30 / 24 / 20 / 17 Ω
  - DDR4 – 240 / 120 / 80 / 60 / 48 / 40 / 34 Ω
  - LPDDR3 – 240 / 120 / 80 / 60 / 48 / 40 / 34 Ω
- Operating frequency up to 1200 MHz (2400 MT/sec) data rate)

Recommended operating conditions

Parameter	Description		Min	Nom	Max	Units
V_{VDD}	Core supply voltage		0.81	0.9	0.99	V
V_{DVDD}	I/O supply voltage	DDR4	1.14	1.2	1.26	V
		DDR3	1.425	1.5	1.575	V
		DDR3L	1.283	1.35	1.45	V
		DDR3U	1.19	1.25	1.31	V
		LPDDR2	1.14	1.2	1.3	V
		LPDDR3	1.14	1.2	1.3	V
T_J	Junction temperature		-40	25	+125	°C
V_{PAD}	Voltage at PAD		V_{DVSS}		V_{DVDD}	V

Characterization Corners

Nominal VDD	Model	VDD	DVDD [1]	Temperature
0.9V	FF	+10%	+10%	-40°C
	FF	+10%	+10%	0°C
	FF	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	0°C
	SS	-10%	-10%	125°C

[1] DVDD = 1.2V, 1.25V, 1.35V, 1.5V
Partial set represented – see datasheet for complete detail.

TSMC28: LPDDR2/3_DDR3/4

Cell summary

Name	Description
SLP_BI_SDS_1215V_D_DVDD/DVSS/PDO *	Bi-directional driver / receiver cell with power
SLP_CL_SDS_1215V_D_PWR *	Differential clock driver / receiver with DVDD / DVSS
SLP_SP_CAL_SDS_1215V *	DDR3 / DDR4 calibration pad
SLP_SP_CSH_0915V *	Calibration code bus driver
SLP_RE_000_1215V *	DDR3 / DDR4 voltage reference
PVP_VD_RCD_0915V	Core power (VDD)
PVP_VS_RCD_0915V	Core ground (VSS)
SVP_SP_000_1215V	0.1 µm spacer
SVP_SP_001_1215V	1 µm spacer
SVP_SP_005_1215V	5 µm spacer
SVP_SP_020_1215V	20 µm spacer
SVP_CO_001_1215V	Corner cell
SPP_RS_005_1215V	Rail splitter
SPP_AD_SSTL_1215V	DDR to staggered 1.8V GPIO adapter
SPP_SP_CAP_1215V	DVDD/DVSS decoupling cap

* Vertical-only and horizontal-only orientations

Physical size

Name	Width	Height	Units
SLP_BI_SDS_1215V_D_DVDD/DVSS/PDO	50	205	µm
SLP_CL_SDS_1215V_D_PWR	100	205	µm
SLP_SP_CAL_SDS_1215V	40	205	µm
SLP_SP_CSH_0915V	20	205	µm
SLP_RE_000_1215V	40	205	µm
PVP_VD_RCD_0915V	25	205	µm
PVP_VS_RCD_0915V	25	205	µm
SVP_SP_000_1215V	0.1	205	µm
SVP_SP_001_1215V	1	205	µm
SVP_SP_005_1215V	5	205	µm
SVP_SP_020_1215V	20	205	µm
SVP_CO_001_1215V	205	205	µm
SPP_RS_005_1215V	5	205	µm
SPP_AD_SSTL_1215V	20	205	µm
SPP_SP_CAP_1215V	10	10	µm

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