TSMC28: LPDDR2/3_DDR3/4



Libraries

Name	Process	Form Factor
RGO_TSMC28_18V15_HPM_25C_LPDDR3_DDR4	HPM	Staggered CUP
RGO_TSMC28_18V15_HPC_25C_LPDDR3_DDR4	HPC	Staggered CUP
RGO_TSMC28_18V15_HPCP_25C_LPDDR3_DDR4	HPC+	Staggered CUP

Summary

The LPDDR2/3_DDR3/4 libraries contain the 6-way combo driver/receiver cells with embedded power cells, the driver impedance calibration cell, and the DDR voltage reference cell providing both single-ended and differential signaling for LPDDR2, LPDDR3, DDR3, DDR3L, DDR3U, and DDR4 applications. Also included is a full complement of power, corner and spacer cells to assemble a complete pad ring by abutment. An included rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

Full DDR4 capability

Data rates – 1600 MT/s, 1866 MT/s, 2133 MT/s, 2400 MT/s

Full DDR3 / DDR3L / DDR3U capability

 Data rates – 800 MT/s, 1066 MT/s, 1333 MT/s, 1600 MT/s, 1866 MT/s, 2133 MT/s

Full LPDDR3 capability

Data rates – 1333 MT/sec, 1600 MT/sec

Full LPDDR2 capability

Data rates – 466 MT/sec, 1066 MT/sec

ESD Protection:

- JEDEC compliant
 - o 2KV ESD Human Body Model (HBM)
 - 200 V ESD Machine Model (MM)
 - 500 V ESD Charge Device Model (CDM)

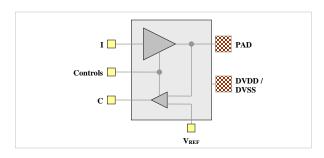
Latch-up Immunity:

- JEDEC compliant
 - o Tested to I-Test criteria of ± 100mA @ 125°C

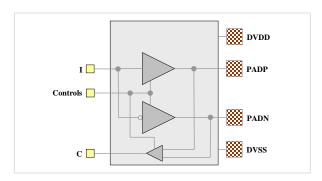
Recommended operating conditions

Parameter	Description		Min	Nom	Max	Units
V _{VDD}	Core supply voltage		0.81	0.9	0.99	V
V _{DVDD}	I/O supply voltage	DDR4	1.14	1.2	1.26	V
		DDR3	1.425	1.5	1.575	V
		DDR3L	1.283	1.35	1.45	V
		DDR3U	1.19	1.25	1.31	V
		LPDDR2	1.14	1.2	1.3	V
		LPDDR3	1.14	1.2	1.3	V
TJ	Junction temperature		-40	25	+125	°C
V _{PAD}	Voltage at PAD		V _{DVSS}		V_{DVDD}	V

SLP_BI_SDS_1215V_D _x: Single-Ended Driver



SLP_CL_SDS_1215V_D_PWR: Differential Driver



Product Features

- User programmable drive strength
 - DDR3 $Z_{OUT} = 34 / 40 \Omega$
 - $\circ \qquad DDR4 Z_{OUT} = 34 \: / \: 48 \: \Omega$
 - o LPDDR2 Z_{OUT} = 34 / 40 / 48 / 60 / 80 Ω
 - $\circ \qquad LPDDR3 Z_{OUT} = 34 / 40 \ \Omega$
- User programmable on-die termination
 - O DDR3 120 / 60 / 40 / 30 / 24 / 20 / 17 Ω
 - O DDR4 240 / 120 / 80 / 60 / 48 / 40 / 34 Ω
- LPDDR3 240 / 120 / 80 / 60 / 48 / 40 / 34 Ω
 Operating frequency up to 1200 MHz (2400 MT/sec) data rate)

TSMC28: LPDDR2/3_DDR3/4 ARAG



Cell summary

Name	Description
SLP_BI_SDS_1215V_D _DVDD/DVSS/PDO *	Bi-directional driver / receiver cell with power
SLP_CL_SDS_1215V_D_PWR *	Differential clock driver / receiver with DVDD / DVSS
SLP_SP_CAL_SDS_1215V *	DDR3 / DDR4 calibration pad
SLP_SP_CSH_0915V *	Calibration code bus driver
SLP_RE_000_1215V *	DDR3 / DDR4 voltage reference
PVP_VD_RCD_0915V	Core power (VDD)
PVP_VS_RCD_0915V	Core ground (VSS)
SVP_SP_000_1215V	0.1 µm spacer
SVP_SP_001_1215V	1 µm spacer
SVP_SP_005_1215V	5 μm spacer
SVP_SP_020_1215V	20 μm spacer
SVP_CO_001_1215V	Corner cell
SPP_RS_005_1215V	Rail splitter
SPP_AD_SSTL_1215V	DDR to staggered 1.8V GPIO adapter
SPP_SP_CAP_1215V	DVDD/DVSS decoupling cap

^{*} Vertical-only and horizontal-only orientations

Characterization Corners (HPM)

Nom VDD	Model	LPE	VDD	DVDD [1]	Temp
	FF	Cbest	+10%	+10%	-40°C
	FF	Cbest	+10%	+10%	0°C
	FF	Cbest	+10%	+10%	125°C
0.9V	FFG	Cworst	+10%	+10%	125°C
	TT	Ctypical	nominal	nominal	25°C
	TT	Ctypical	nominal	nominal	85°C
	SSG	Cworst	-10%	-10%	-40°C
	SSG	Cworst	-10%	-10%	0°C
	SSG	Cworst	-10%	-10%	125°C

[1] DVDD = 1.2V, 1.25V, 1.35V, 1.5V

Characterization Corners (HPC)

Nom VDD	Model	LPE	VDD	DVDD [1]	Temp
	FF	Cbest	+10%	+10%	-40°C
	FF	Cbest	+10%	+10%	0°C
	FF	Cbest	+10%	+10%	125°C
	FFG	Cworst	+10%	+10%	125°C
0.9V	TT	Ctypical	nominal	nominal	25°C
	TT	Ctypical	nominal	nominal	85°C
	SS	Cworst	-10%	-10%	-40°C
	SS	Cworst	-10%	-10%	0°C
	SS	Cworst	-10%	-10%	125°C

[1] DVDD = 1.2V, 1.25V, 1.35V, 1.5V

Physical size

Name	Width	Height	Units
SLP_BI_SDS_1215V_D _DVDD/DVSS/PDO	50	205	μm
SLP_CL_SDS_1215V_D_PWR	100	205	μm
SLP_SP_CAL_SDS_1215V	40	205	μm
SLP_SP_CSH_0915V	20	205	μm
SLP_RE_000_1215V	40	205	μm
PVP_VD_RCD_0915V	25	205	μm
PVP_VS_RCD_0915V	25	205	μm
SVP_SP_000_1215V	0.1	205	μm
SVP_SP_001_1215V	1	205	μm
SVP_SP_005_1215V	5	205	μm
SVP_SP_020_1215V	20	205	μm
SVP_CO_001_1215V	205	205	μm
SPP_RS_005_1215V	5	205	μm
SPP_AD_SSTL_1215V	20	205	μm
SPP_SP_CAP_1215V	10	10	μm

Characterization Corners (HPC+)

Nom VDD	Model	LPE	VDD	DVDD [1]	Temp
	FFG	Cbest	+10%	+10%	-40°C
	FFG	Cbest	+10%	+10%	0°C
0.9V	FFG	Cbest	+10%	+10%	125°C
	TT	Ctypical	nominal	nominal	25°C
	TT	Ctypical	nominal	nominal	85°C
	SSG	Cworst	-10%	-10%	-40°C
	SSG	Cworst	-10%	-10%	0°C
	SSG	Cworst	-10%	-10%	125°C

[1] DVDD = 1.2V, 1.25V, 1.35V, 1.5V

© 2011-2017 Aragio Solutions. All rights reserved.

Information in this document is subject to change without notice. Aragio Solutions may have patents, patent applications, trademarks, copyrights or other intellectual property rights covering subject matter in this document. Except as expressly provided in any written license agreement from Aragio, the furnishing of this document does not give you any license to the patents, trademarks, copyrights, or other intellectual property.

Published by:

Aragio Solutions 2201 K Avenue Section B Suite 200 Plano, TX 75074-5918

(972) 516-0999 Phone: (972) 516-0998 Fax: Web: http://www.aragio.com/

While every precaution has been taken in the preparation of this book, the publisher assumes no responsibility for errors or omissions, or for damages resulting from the use of the information contained herein. This document may be reproduced and distributed in whole, in any medium, physical or electronic, under the terms of a license or nondisclosure agreement with Aragio.

Printed in the United States of America